



8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10V$, $\pm 5V$, and 0 to +5V Analog Input Ranges

General Description

The MAX1304–MAX1306/MAX1308–MAX1310/MAX1312–MAX1314 12-bit, analog-to-digital converters (ADCs) offer eight, four, or two independent input channels. Independent track-and-hold (T/H) circuitry provides simultaneous sampling for each channel. The MAX1304/MAX1305/MAX1306 provide a 0 to +5V input range with $\pm 6V$ fault-tolerant inputs. The MAX1308/MAX1309/MAX1310 provide a $\pm 5V$ input range with $\pm 16.5V$ fault-tolerant inputs. The MAX1312/MAX1313/MAX1314 have a $\pm 10V$ input range with $\pm 16.5V$ fault-tolerant inputs. These ADCs convert two channels in 0.9 μ s, and up to eight channels in 1.98 μ s, with an 8-channel throughput of 456ksps per channel. Other features include a 20MHz T/H input bandwidth, internal clock, internal (+2.5V) or external (+2.0V to +3.0V) reference, and power-saving modes.

A 20MHz, 12-bit, bidirectional parallel data bus provides the conversion results and accepts digital inputs that activate each channel individually.

All devices operate from a +4.75V to +5.25V analog supply and a +2.7V to +5.25V digital supply and consume 57mA total supply current when fully operational.

Each device is available in a 48-pin 7mm x 7mm TQFP package and operates over the extended -40°C to +85°C temperature range.

Applications

SIN/COS Position Encoder
Multiphase Motor Control
Multiphase Power Monitoring
Power-Grid Synchronization
Power-Factor Monitoring
Vibration and Waveform Analysis

Selector Guide

PART	INPUT RANGE (V)	CHANNEL COUNT
MAX1304ECM	0 to +5	8
MAX1305ECM	0 to +5	4
MAX1306ECM	0 to +5	2
MAX1308ECM	± 5	8
MAX1309ECM	± 5	4
MAX1310ECM	± 5	2
MAX1312ECM	± 10	8
MAX1313ECM	± 10	4
MAX1314ECM	± 10	2

Pin Configurations appear at end of data sheet.

Features

- ◆ Up to Eight Channels of Simultaneous Sampling
8ns Aperture Delay
100ps Channel-to-Channel T/H Match
- ◆ Extended Input Ranges
0 to +5V (MAX1304/MAX1305/MAX1306)
-5V to +5V (MAX1308/MAX1309/MAX1310)
-10V to +10V (MAX1312/MAX1313/MAX1314)
- ◆ Fast Conversion Time
One Channel in 0.72 μ s
Two Channels in 0.9 μ s
Four Channels in 1.26 μ s
Eight Channels in 1.98 μ s
- ◆ High Throughput
1075ksps/Channel for One Channel
901ksps/Channel for Two Channels
680ksps/Channel for Four Channels
456ksps/Channel for Eight Channels
- ◆ ± 1 LSB INL, ± 0.9 LSB DNL (max)
- ◆ 84dBc SFDR, -86dBc THD, 71dB SINAD,
 $f_{IN} = 500kHz$ at 0.4dBFS
- ◆ 12-Bit, 20MHz, Parallel Interface
- ◆ Internal or External Clock
- ◆ +2.5V Internal Reference or +2.0V to +3.0V
External Reference
- ◆ +5V Analog Supply, +3V to +5V Digital Supply
55mA Analog Supply Current
1.3mA Digital Supply Current
Shutdown and Power-Saving Modes
- ◆ 48-Pin TQFP Package (7mm x 7mm Footprint)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1304ECM	-40°C to +85°C	48 TQFP
MAX1305ECM	-40°C to +85°C	48 TQFP
MAX1306ECM	-40°C to +85°C	48 TQFP
MAX1308ECM	-40°C to +85°C	48 TQFP
MAX1309ECM	-40°C to +85°C	48 TQFP
MAX1310ECM	-40°C to +85°C	48 TQFP
MAX1312ECM	-40°C to +85°C	48 TQFP
MAX1313ECM	-40°C to +85°C	48 TQFP
MAX1314ECM	-40°C to +85°C	48 TQFP

MAX1304-MAX1306/MAX1308-MAX1310/MAX1312-MAX1314



8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

ABSOLUTE MAXIMUM RATINGS

AV _{DD} to AGND	-0.3V to +6V	REF _{MS} , REF, MSV to AGND	-0.3V to (AV _{DD} + 0.3V)
DV _{DD} to DGND	-0.3V to +6V	REF+, COM, REF- to AGND	-0.3V to (AV _{DD} + 0.3V)
AGND to DGND	-0.3V to +0.3V	Maximum Current into Any Pin Except AV _{DD} , DV _{DD} , AGND, DGND	±50mA
CH0-CH7, I.C. to AGND (MAX1304/MAX1305/MAX1306)	±6V	Continuous Power Dissipation (T _A = +70°C)	
CH0-CH7, I.C. to AGND (MAX1308/MAX1309/MAX1310)	±16.5V	TQFP (derate 22.7mW/°C above +70°C)	1818.2mW
CH0-CH7, I.C. to AGND (MAX1312/MAX1313/MAX1314)	±16.5V	Operating Temperature Range	-40°C to +85°C
D0-D11 to DGND	-0.3V to (DV _{DD} + 0.3V)	Junction Temperature	+150°C
E _{OC} , E _{OLC} , RD, WR, CS to DGND	-0.3V to (DV _{DD} + 0.3V)	Storage Temperature Range	-65°C to +150°C
CONVST, CLK, SHDN, CHSHDN to DGND	-0.3V to (DV _{DD} + 0.3V)	Lead Temperature (soldering, 10s)	+300°C
INTCLK/EXTCLK to AGND	-0.3V to (AV _{DD} + 0.3V)		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = +5V, DV_{DD} = +3V, AGND = DGND = 0, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1μF, C_{REF+} = C_{REF-} = 0.1μF, C_{REF+to-REF-} = 2.2μF || 0.1μF, C_{COM} = 2.2μF || 0.1μF, C_{MSV} = 2.2μF || 0.1μF (unipolar devices), MSV = AGND (bipolar devices), f_{CLK} = 16.67MHz 50% duty cycle, INTCLK/EXTCLK = AGND (external clock), SHDN = DGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. See Figures 3 and 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Note 1)						
Resolution	N		12			Bits
Integral Nonlinearity	INL	(Note 2)		±0.5	±1.0	LSB
Differential Nonlinearity	DNL	No missing codes (Note 2)		±0.3	±0.9	LSB
Offset Error		Unipolar, 0x000 to 0x001		±3	±16	LSB
		Bipolar, 0xFFFF to 0x000		±3	±16	
Offset-Error Matching		Unipolar, between all channels		±9	±20	LSB
		Bipolar, between all channels		±9	±20	
Offset-Error Temperature Drift		Unipolar, 0x000 to 0x001		7		ppm/°C
		Bipolar, 0xFFFF to 0x000		7		
Gain Error				±2	±16	LSB
Gain-Error Matching		Between all channels		±3	±14	LSB
Gain-Error Temperature Drift				4		ppm/°C
DYNAMIC PERFORMANCE at f_{IN} = 500kHz, A_{IN} = -0.4dBFS (Note 2)						
Signal-to-Noise Ratio	SNR		68	71		dB
Signal-to-Noise Plus Distortion	SINAD		68	71		dB
Total Harmonic Distortion	THD			-86	-80	dBc
Spurious-Free Dynamic Range	SFDR			84		dBc
Channel-to-Channel Isolation			80	86		dB
ANALOG INPUTS (CH0 through CH7)						
Input Voltage	V _{CH}	MAX1304/MAX1305/MAX1306	0		+5	V
		MAX1308/MAX1309/MAX1310	-5		+5	
		MAX1312/MAX1313/MAX1314	-10		+10	

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

MAX1304-MAX1306/MAX1308-MAX1310/MAX1312-MAX1314

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = +5V, DVDD = +3V, AGND = DGND = 0, VREF = VREFMS = +2.5V (external reference), CREF = CREFMS = 0.1μF, CREF+ = CREF- = 0.1μF, CREF+to-REF- = 2.2μF || 0.1μF, CCOM = 2.2μF || 0.1μF, CMSV = 2.2μF || 0.1μF (unipolar devices), MSV = AGND (bipolar devices), fCLK = 16.67MHz 50% duty cycle, INTCLK/EXTCLK = AGND (external clock), SHDN = DGND, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C. See Figures 3 and 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Resistance (Note 3)	RCH	MAX1304/MAX1305/MAX1306		7.58		kΩ
		MAX1308/MAX1309/MAX1310		8.66		
		MAX1312/MAX1313/MAX1314		14.26		
Input Current (Note 3)	ICH	MAX1304/MAX1305/MAX1306	VCH = +5V	0.54	0.72	mA
			VCH = 0V	-0.157	-0.12	
		MAX1308/MAX1309/MAX1310	VCH = +5V	0.29	0.39	
			VCH = -5V	-1.16	-0.87	
		MAX1312/MAX1313/MAX1314	VCH = +10V	0.56	0.74	
			VCH = -10V	-1.13	-0.85	
Input Capacitance	CCH			15		pF
TRACK/HOLD						
External-Clock Throughput Rate (Note 4)	fTH	One channel selected for conversion		1075		ksp/s
		Two channels selected for conversion		901		
		Four channels selected for conversion		680		
		Eight channels selected for conversion		456		
Internal-Clock Throughput Rate (Note 4, Table 1)	fTH	One channel selected for conversion		983		ksp/s
		Two channels selected for conversion		821		
		Four channels selected for conversion		618		
		Eight channels selected for conversion		413		
Small-Signal Bandwidth				20		MHz
Full-Power Bandwidth				20		MHz
Aperture Delay	tAD			8		ns
Aperture-Delay Matching				100		ps
Aperture Jitter	tAJ			50		psRMS
INTERNAL REFERENCE						
REF Output Voltage	VREF		2.475	2.500	2.525	V
Reference Output-Voltage Temperature Drift				30		ppm/°C
REFMS Output Voltage	VREFMS		2.475	2.500	2.525	V
REF+ Output Voltage	VREF+			3.850		V
COM Output Voltage	VCOM			2.600		V
REF- Output Voltage	VREF-			1.350		V
Differential Reference Voltage	VREF+ - VREF-			2.500		V

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10V$, $\pm 5V$, and 0 to +5V Analog Input Ranges

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = +5V, DVDD = +3V, AGND = DGND = 0, VREF = VREFMS = +2.5V (external reference), CREF = CREFMS = 0.1 μ F, CREF+ = CREF- = 0.1 μ F, CREF+to-REF- = 2.2 μ F || 0.1 μ F, CCOM = 2.2 μ F || 0.1 μ F, CMSV = 2.2 μ F || 0.1 μ F (unipolar devices), MSV = AGND (bipolar devices), fCLK = 16.67MHz 50% duty cycle, INTCLK/EXTCLK = AGND (external clock), SHDN = DGND, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C. See Figures 3 and 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE (REF and REFMS are externally driven)						
REF Input Voltage Range	VREF		2.0	2.5	3.0	V
REF Input Resistance	RREF	(Note 5)		5		k Ω
REF Input Capacitance				15		pF
REFMS Input Voltage Range	VREFMS		2.0	2.5	3.0	V
REFMS Input Resistance	RREFMS	(Note 6)		5		k Ω
REFMS Input Capacitance				15		pF
REF+ Output Voltage	VREF+	VREF = +2.5V		3.850		V
COM Output Voltage	VCOM	VREF = +2.5V		2.600		V
REF- Output Voltage	VREF-	VREF = +2.5V		1.350		V
Differential Reference Voltage	VREF+ - VREF-	VREF = +2.5V		2.500		V
DIGITAL INPUTS (D0-D7, RD, WR, CS, CLK, SHDN, CHSHDN, CONVST)						
Input-Voltage High	VIH		0.7 x DVDD			V
Input-Voltage Low	VIL		0.3 x DVDD			V
Input Hysteresis			20			mV
Input Capacitance	CIN		15			pF
Input Current	IIN	VIN = 0 or DVDD	0.02	± 1		μ A
CLOCK-SELECT INPUT (INTCLK/EXTCLK)						
Input-Voltage High	VIH		0.7 x AVDD			V
Input-Voltage Low	VIL		0.3 x AVDD			V
DIGITAL OUTPUTS (D0-D11, EOC, EOLC)						
Output-Voltage High	VOH	ISOURCE = 0.8mA, Figure 1	DVDD - 0.6			V
Output-Voltage Low	VOL	ISINK = 1.6mA, Figure 1	0.4			V
D0-D11 Tri-State Leakage Current		RD = high or CS = high	0.06	1		μ A
D0-D11 Tri-State Output Capacitance		RD = high or CS = high	15			pF
POWER SUPPLIES						
Analog Supply Voltage	AVDD		4.75	5.25		V
Digital Supply Voltage	DVDD		2.70	5.25		V
Analog Supply Current	IAVDD	MAX1304/MAX1305/MAX1306, all channels selected	55	60		mA
		MAX1308/MAX1309/MAX1310, all channels selected	54	60		
		MAX1312/MAX1313/MAX1314, all channels selected	54	60		

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = +5V, DVDD = +3V, AGND = DGND = 0, VREF = VREFMS = +2.5V (external reference), CREF = CREFMS = 0.1μF, CREF+ = CREF- = 0.1μF, CREF+to-REF- = 2.2μF || 0.1μF, CCOM = 2.2μF || 0.1μF, CMSV = 2.2μF || 0.1μF (unipolar devices), MSV = AGND (bipolar devices), fCLK = 16.67MHz 50% duty cycle, INTCLK/EXTCLK = AGND (external clock), SHDN = DGND, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C. See Figures 3 and 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Current (CLOAD = 100pF) (Note 7)	IDVDD	MAX1304/MAX1305/MAX1306, all channels selected		1.3	2.6	mA
		MAX1308/MAX1309/MAX1310, all channels selected		1.3	2.6	
		MAX1312/MAX1313/MAX1314, all channels selected		1.3	2.6	
Shutdown Current (Note 8)	IAVDD	SHDN = DVDD, VCH = float		0.6	10	μA
	IDVDD	SHDN = DVDD, $\overline{RD} = \overline{WR} = \text{high}$		0.02	1	
Power-Supply Rejection Ratio	PSRR	AVDD = +4.75V to +5.25V		50		dB
TIMING CHARACTERISTICS (Figure 1)						
Time to First Conversion Result	tCONV	Internal clock, Figure 7		800	900	ns
		External clock, Figure 8		12		CLK Cycles
Time to Subsequent Conversions	tNEXT	Internal clock, Figure 7		200	225	ns
		External clock, Figure 8		3		CLK Cycles
CONVST Pulse-Width Low (Acquisition Time)	tACQ	(Note 9) Figures 6–10	0.1		1000.0	μs
\overline{CS} Pulse Width	tCS	Figure 6	30			ns
\overline{RD} Pulse-Width Low	tRDL	Figures 7, 8, 9	30			ns
\overline{RD} Pulse-Width High	tRDH	Figures 7, 8, 9	30			ns
\overline{WR} Pulse-Width Low	tWRL	Figure 6	30			ns
\overline{CS} to \overline{WR}	tCTW	Figure 6		(Note 10)		ns
\overline{WR} to \overline{CS}	tWTC	Figure 6		(Note 10)		ns
\overline{CS} to \overline{RD}	tCTR	Figures 7, 8, 9		(Note 10)		ns
\overline{RD} to \overline{CS}	tRTC	Figures 7, 8, 9		(Note 10)		ns
Data Access Time (\overline{RD} Low to Valid Data)	tACC	Figures 7, 8, 9			30	ns
Bus Relinquish Time (\overline{RD} High)	tREQ	Figures 7, 8, 9	5		30	ns
CLK Rise to \overline{EOC} Delay	tEOCD	Figure 8		20		ns
CLK Rise to \overline{EOLC} Fall Delay	tEOLCD	Figure 8		20		ns
CONVST Fall to \overline{EOLC} Rise Delay	tcVEOLCD	Figures 7, 8, 9		20		ns
\overline{EOC} Pulse Width	tEOC	Internal clock, Figure 7	50			ns
		External clock, Figure 8		1		CLK Cycle

MAX1304-MAX1306/MAX1308-MAX1310/MAX1312-MAX1314

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10V$, $\pm 5V$, and 0 to +5V Analog Input Ranges

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = +5V, DVDD = +3V, AGND = DGND = 0, VREF = VREFMS = +2.5V (external reference), CREF = CREFMS = 0.1 μ F, CREF+ = CREF- = 0.1 μ F, CREF+to-REF- = 2.2 μ F || 0.1 μ F, CCOM = 2.2 μ F || 0.1 μ F, CMSV = 2.2 μ F || 0.1 μ F (unipolar devices), MSV = AGND (bipolar devices), fCLK = 16.67MHz 50% duty cycle, INTCLK/EXTCLK = AGND (external clock), SHDN = DGND, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C. See Figures 3 and 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Data Setup Time	tDTW	Figure 6	10			ns
Input-Data Hold Time	tWTD	Figure 6	10			ns
External CLK Period	tCLK	Figures 8, 9	0.05		10.00	μ s
External CLK High Period	tCLKH	Logic sensitive to rising edges, Figures 8, 9	20			ns
External CLK Low Period	tCLKL	Logic sensitive to rising edges, Figures 8, 9	20			ns
External Clock Frequency	fCLK	(Note 11)	0.1		20	MHz
Internal Clock Frequency	fINT			15		MHz
CONVST High to CLK Edge	tCNTC	Figures 8, 9	20			ns

Note 1: For the MAX1304/MAX1305/MAX1306, VIN = 0 to +5V. For the MAX1308/MAX1309/MAX1310, VIN = -5V to +5V. For the MAX1312/MAX1313/MAX1314, VIN = -10V to +10V.

Note 2: All channel performance is guaranteed by correlation to a single channel test.

Note 3: The analog input resistance is terminated to an internal bias point (Figure 5). Calculate the analog input current using:

$$I_{CH_} = \frac{V_{CH_} - V_{BIAS}}{R_{CH_}}$$

for VCH within the input voltage range.

Note 4: Throughput rate is given per channel. Throughput rate is a function of clock frequency (fCLK). The external clock throughput rate is specified with fCLK = 16.67MHz and the internal clock throughput rate is specified with fCLK = 15MHz. See the *Data Throughput* section for more information.

Note 5: The REF input resistance is terminated to an internal +2.5V bias point (Figure 2). Calculate the REF input current using:

$$I_{REF} = \frac{V_{REF} - 2.5V}{R_{REF}}$$

for VREF within the input voltage range.

Note 6: The REFMS input resistance is terminated to an internal +2.5V bias point (Figure 2). Calculate the REFMS input current using:

$$I_{REFMS} = \frac{V_{REFMS} - 2.5V}{R_{REFMS}}$$

for VREFMS within the input voltage range.

Note 7: All analog inputs are driven with a -0.4dBFS 500kHz sine wave.

Note 8: Shutdown current is measured with the analog input floating. The large amplitude of the maximum shutdown current specification is due to automated test equipment limitations.

Note 9: CONVST must remain low for at least the acquisition period. The maximum acquisition time is limited by internal capacitor droop.

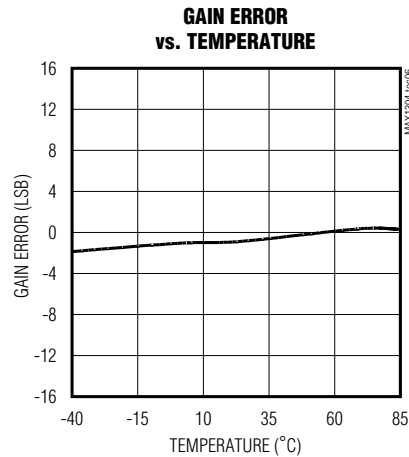
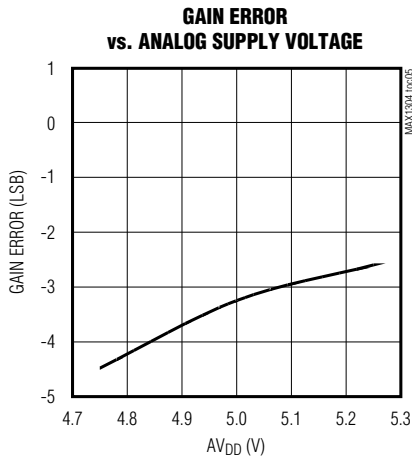
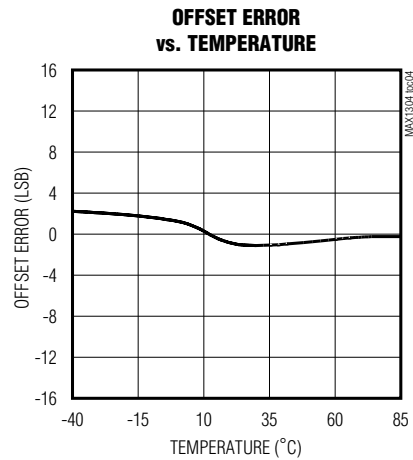
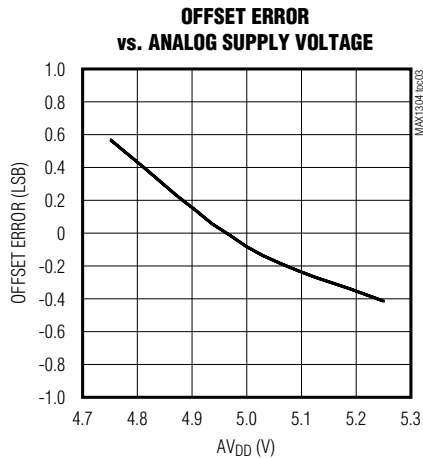
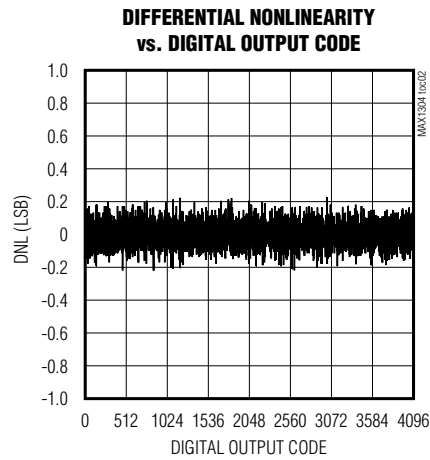
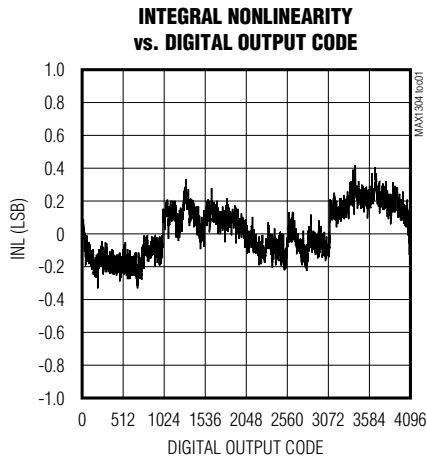
Note 10: CS to WR and CS to RD are internally AND together. Setup and hold times do not apply.

Note 11: Minimum CLK frequency is limited only by the internal T/H droop rate. Limit the time between the rising edge of CONVST and the falling edge of EOLC to a maximum of 1ms.

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Typical Operating Characteristics

($A_{VDD} = +5V$, $DV_{DD} = +3V$, $AGND = DGND = 0$, $V_{REF} = V_{REFMS} = +2.5V$ (external reference), $C_{REF} = C_{REFMS} = 0.1\mu F$, $C_{REF+} = C_{REF-} = 0.1\mu F$, $C_{REF+to-REF-} = 2.2\mu F \parallel 0.1\mu F$, $C_{COM} = 2.2\mu F \parallel 0.1\mu F$, $C_{MSV} = 2.2\mu F \parallel 0.1\mu F$ (unipolar devices), $MSV = AGND$ (bipolar devices), $f_{CLK} = 16.67MHz$ 50% duty cycle, $INTCLK/EXTCLK = AGND$ (external clock), $f_{IN} = 500kHz$, $A_{IN} = -0.4dBFS$. $T_A = +25^\circ C$, unless otherwise noted.) (Figures 3 and 4)

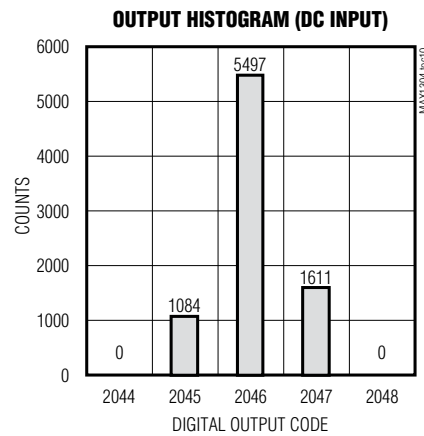
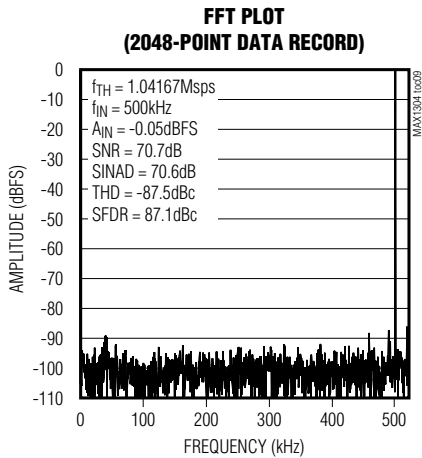
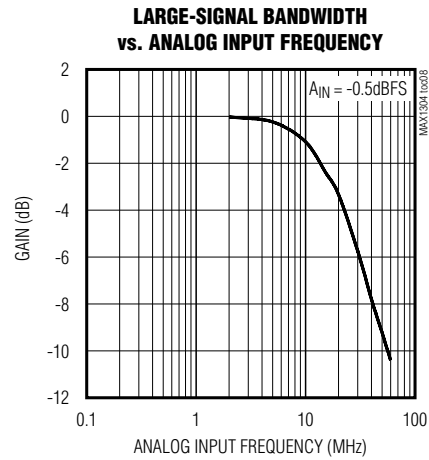
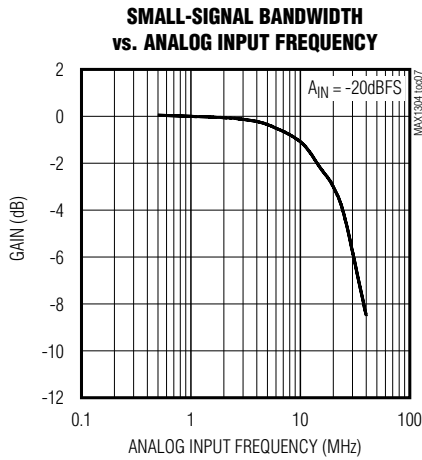


MAX1304-MAX1306/MAX1308-MAX1310/MAX1312-MAX1314

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

Typical Operating Characteristics (continued)

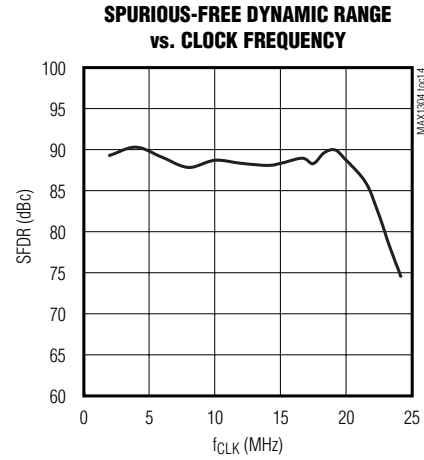
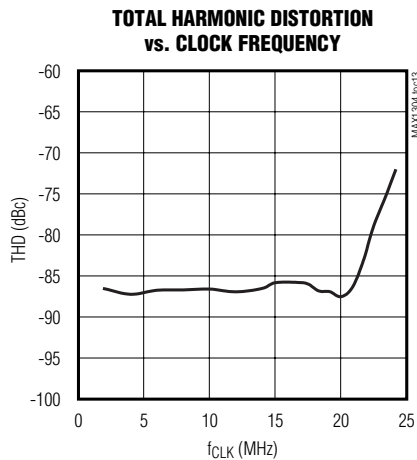
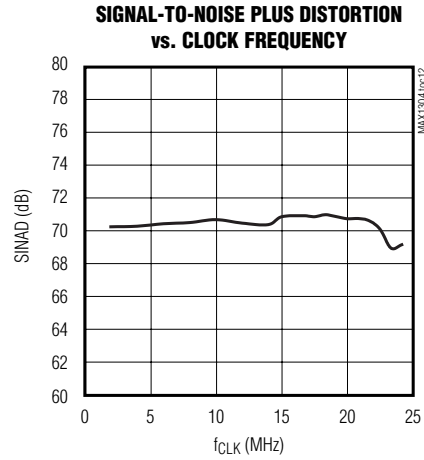
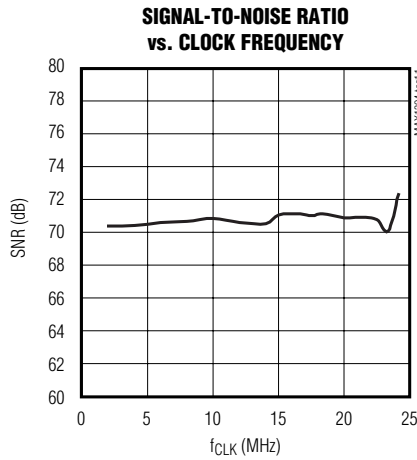
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8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10V$, $\pm 5V$, and 0 to +5V Analog Input Ranges

Typical Operating Characteristics (continued)

($V_{DD} = +5V$, $DV_{DD} = +3V$, $AGND = DGND = 0$, $V_{REF} = V_{REFMS} = +2.5V$ (external reference), $C_{REF} = C_{REFMS} = 0.1\mu F$, $C_{REF+} = C_{REF-} = 0.1\mu F$, $C_{REF+to-REF-} = 2.2\mu F \parallel 0.1\mu F$, $C_{COM} = 2.2\mu F \parallel 0.1\mu F$, $C_{MSV} = 2.2\mu F \parallel 0.1\mu F$ (unipolar devices), $MSV = AGND$ (bipolar devices), $f_{CLK} = 16.67MHz$ 50% duty cycle, $INTCLK/EXTCLK = AGND$ (external clock), $f_{IN} = 500kHz$, $A_{IN} = -0.4dBFS$. $T_A = +25^\circ C$, unless otherwise noted.) (Figures 3 and 4)

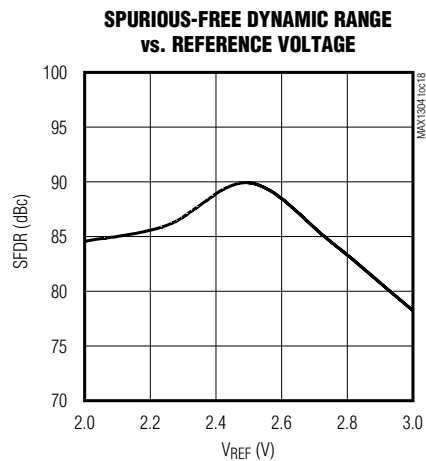
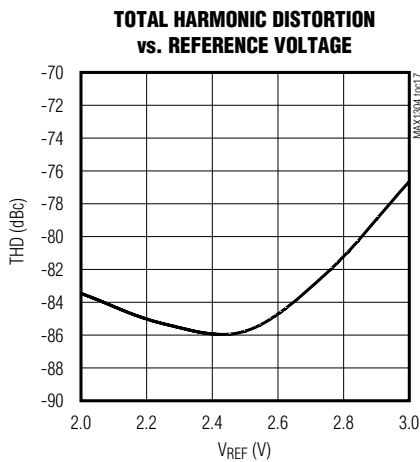
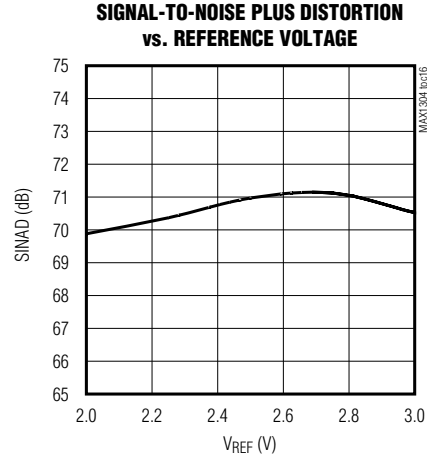
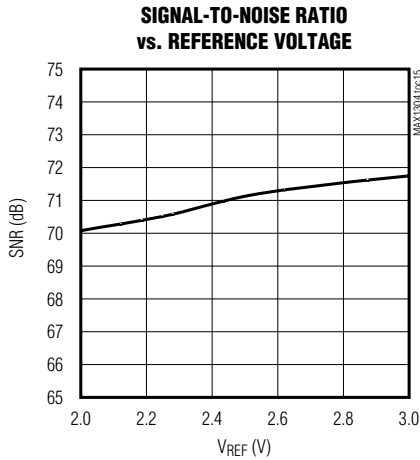


MAX1304-MAX1306-MAX1308-MAX1310-MAX1312-MAX1314

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

Typical Operating Characteristics (continued)

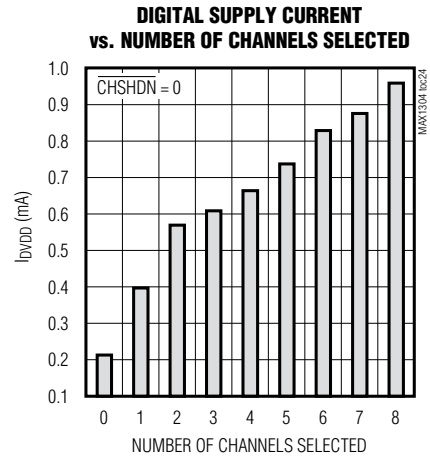
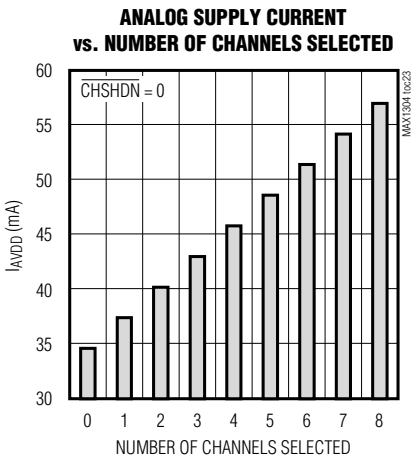
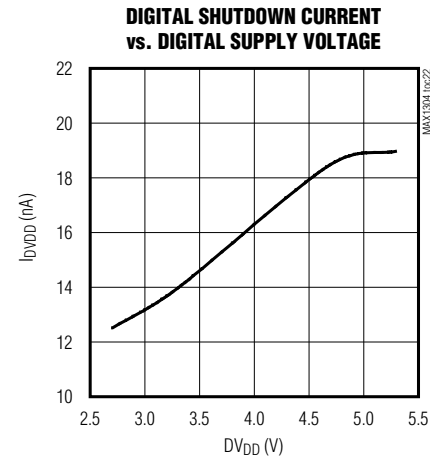
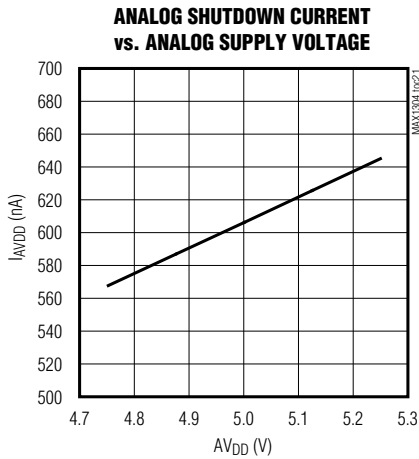
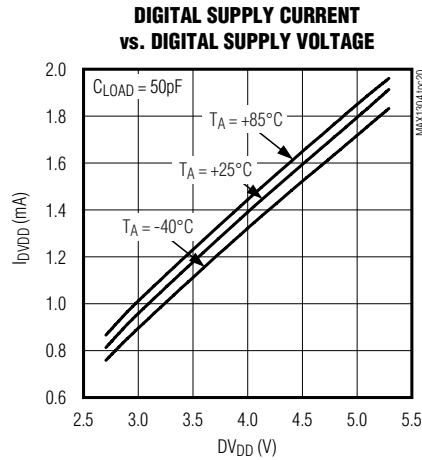
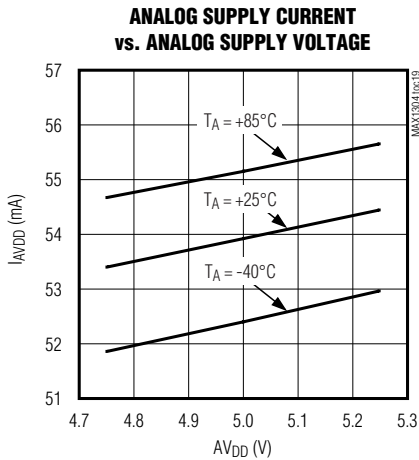
(AVDD = +5V, DVDD = +3V, AGND = DGND = 0, VREF = VREFMS = +2.5V (external reference), CREF = CREFMS = 0.1μF, CREF+ = CREF- = 0.1μF, CREF+to-REF- = 2.2μF || 0.1μF, CCOM = 2.2μF || 0.1μF, CMSV = 2.2μF || 0.1μF (unipolar devices), MSV = AGND (bipolar devices), fCLK = 16.67MHz 50% duty cycle, INTCLK/EXTCLK = AGND (external clock), fIN = 500kHz, AIN = -0.4dBFS. TA = +25°C, unless otherwise noted.) (Figures 3 and 4)



8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

Typical Operating Characteristics (continued)

(AVDD = +5V, DVDD = +3V, AGND = DGND = 0, VREF = VREFMS = +2.5V (external reference), CREF = CREFMS = 0.1μF, CREF+ = CREF- = 0.1μF, CREF+to-REF- = 2.2μF || 0.1μF, CCOM = 2.2μF || 0.1μF, CMSV = 2.2μF || 0.1μF (unipolar devices), MSV = AGND (bipolar devices), fCLK = 16.67MHz 50% duty cycle, INTCLK/EXTCLK = AGND (external clock), fIN = 500kHz, AIN = -0.4dBFS. TA = +25°C, unless otherwise noted.) (Figures 3 and 4)

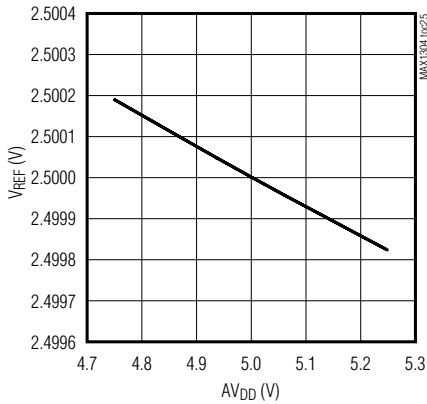


8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

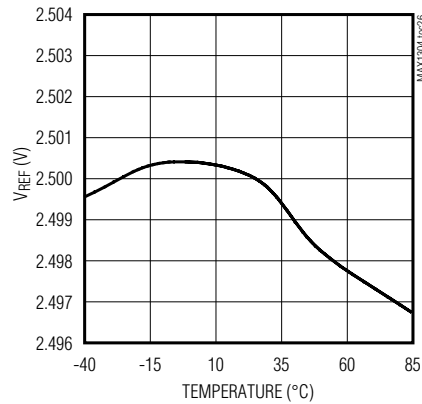
Typical Operating Characteristics (continued)

(AVDD = +5V, DVDD = +3V, AGND = DGND = 0, VREF = VREFMS = +2.5V (external reference), CREF = CREFMS = 0.1μF, CREF+ = CREF- = 0.1μF, CREF+to-REF- = 2.2μF || 0.1μF, CCOM = 2.2μF || 0.1μF, CMSV = 2.2μF || 0.1μF (unipolar devices), MSV = AGND (bipolar devices), fCLK = 16.67MHz 50% duty cycle, INTCLK/EXTCLK = AGND (external clock), fIN = 500kHz, AIN = -0.4dBFS. TA = +25°C, unless otherwise noted.) (Figures 3 and 4)

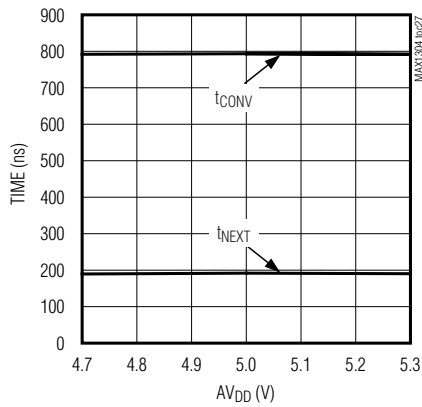
INTERNAL REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



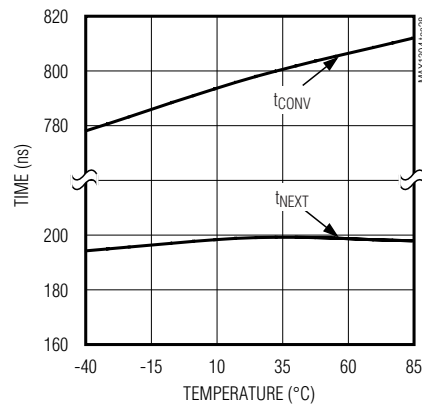
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



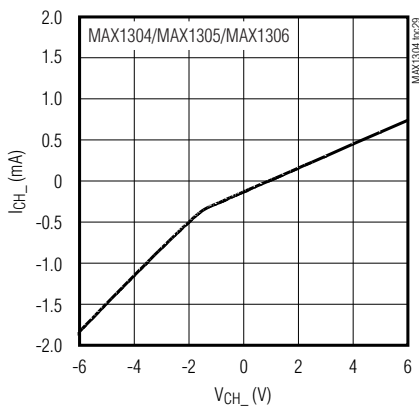
INTERNAL CLOCK CONVERSION TIME vs. ANALOG SUPPLY VOLTAGE



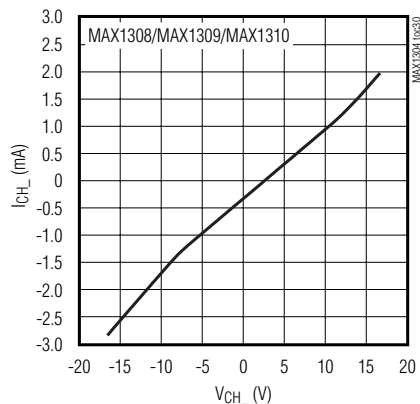
INTERNAL CLOCK CONVERSION TIME vs. TEMPERATURE



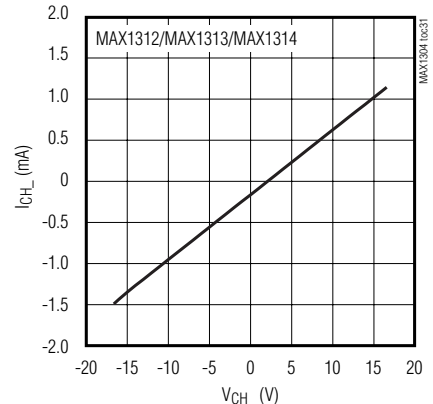
ANALOG INPUT CHANNEL CURRENT vs. ANALOG INPUT CHANNEL VOLTAGE



ANALOG INPUT CHANNEL CURRENT vs. ANALOG INPUT CHANNEL VOLTAGE



ANALOG INPUT CHANNEL CURRENT vs. ANALOG INPUT CHANNEL VOLTAGE



8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10V$, $\pm 5V$, and 0 to +5V Analog Input Ranges

Pin Description

PIN			NAME	FUNCTION
MAX1304 MAX1308 MAX1312	MAX1305 MAX1309 MAX1313	MAX1306 MAX1310 MAX1314		
1, 15, 17	1, 15, 17	1, 15, 17	AVDD	Analog Power Input. AVDD is the power input for the analog section of the converter. Apply +5V to AVDD. Connect all AVDD pins together. See the <i>Layout, Grounding, and Bypassing</i> section for additional information.
2, 3, 14, 16, 23	2, 3, 14, 16, 23	2, 3, 14, 16, 23	AGND	Analog Ground. AGND is the power return for AVDD. Connect all AGND pins together.
4	4	4	CH0	Channel 0 Analog Input
5	5	5	CH1	Channel 1 Analog Input
6	6	6	MSV	Midscale Voltage Bypass. For the unipolar MAX1304/MAX1305/MAX1306, connect a 2.2 μ F and a 0.1 μ F capacitor from MSV to AGND. For the bipolar MAX1308/MAX1309/MAX1310/MAX1312/MAX1313/MAX1314, connect MSV to AGND.
7	7	—	CH2	Channel 2 Analog Input
8	8	—	CH3	Channel 3 Analog Input
9	—	—	CH4	Channel 4 Analog Input
10	—	—	CH5	Channel 5 Analog Input
11	—	—	CH6	Channel 6 Analog Input
12	—	—	CH7	Channel 7 Analog Input
13	13	13	INTCLK/ EXTCLK	Clock-Mode Select Input. Connect INTCLK/EXTCLK to AVDD to select the internal clock. Connect INTCLK/EXTCLK to AGND to use an external clock connected to CLK.
18	18	18	REFMS	Midscale Reference Bypass or Input. REFMS connects through a 5k Ω resistor to the internal +2.5V bandgap reference buffer. For the MAX1304/MAX1305/MAX1306 unipolar devices, VREFMS is the input to the unity-gain buffer that drives MSV. MSV sets the midpoint of the input voltage range. For internal reference operation, bypass REFMS with a $\geq 0.01\mu$ F capacitor to AGND. For external reference operation, drive REFMS with an external voltage from +2V to +3V. For the MAX1308/MAX1309/MAX1310/MAX1312/MAX1313/MAX1314 bipolar devices, connect REFMS to REF. For internal reference operation, bypass the REFMS/REF node with a $\geq 0.01\mu$ F capacitor to AGND. For external reference operation, drive the REFMS/REF node with an external voltage from +2V to +3V.
19	19	19	REF	ADC Reference Bypass or Input. REF connects through a 5k Ω resistor to the internal +2.5V bandgap reference buffer. For internal reference operation, bypass REF with a $\geq 0.01\mu$ F capacitor. For external reference operation with the MAX1304/MAX1305/MAX1306 unipolar devices, drive REF with an external voltage from +2V to +3V. For external reference operation with the MAX1308/MAX1309/MAX1310/MAX1312/MAX1313/MAX1314 bipolar devices, connect REFMS to REF and drive the REFMS/REF node with an external voltage from +2V to +3V.

MAX1304-MAX1306/MAX1308-MAX1310/MAX1312-MAX1314

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10V$, $\pm 5V$, and 0 to +5V Analog Input Ranges

Pin Description (continued)

PIN			NAME	FUNCTION
MAX1304 MAX1308 MAX1312	MAX1305 MAX1309 MAX1313	MAX1306 MAX1310 MAX1314		
20	20	20	REF+	Positive Reference Bypass. Bypass REF+ with a 0.1 μ F capacitor to AGND. Also bypass REF+ to REF- with a 2.2 μ F and a 0.1 μ F capacitor. $V_{REF+} = V_{COM} + V_{REF} / 2$.
21	21	21	COM	Reference Common Bypass. Bypass COM to AGND with a 2.2 μ F and a 0.1 μ F capacitor. $V_{COM} = 13 / 25 \times AV_{DD}$.
22	22	22	REF-	Negative Reference Bypass. Bypass REF- with a 0.1 μ F capacitor to AGND. Also bypass REF- to REF+ with a 2.2 μ F and a 0.1 μ F capacitor. $V_{REF+} = V_{COM} - V_{REF} / 2$.
24, 39	24, 39	24, 39	DGND	Digital Ground. DGND is the power return for DV _{DD} . Connect all DGND pins together.
25, 38	25, 38	25, 38	DV _{DD}	Digital Power Input. DV _{DD} powers the digital section of the converter, including the parallel interface. Apply +2.7V to +5.25V to DV _{DD} . Bypass DV _{DD} to DGND with a 0.1 μ F capacitor. Connect all DV _{DD} pins together.
26	26	26	D0	Digital I/O 0 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD} = 1$ or $\overline{CS} = 1$.
27	27	27	D1	Digital I/O 1 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD} = 1$ or $\overline{CS} = 1$.
28	28	28	D2	Digital I/O 2 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD} = 1$ or $\overline{CS} = 1$.
29	29	29	D3	Digital I/O 3 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD} = 1$ or $\overline{CS} = 1$.
30	30	30	D4	Digital I/O 4 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD} = 1$ or $\overline{CS} = 1$.
31	31	31	D5	Digital I/O 5 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD} = 1$ or $\overline{CS} = 1$.
32	32	32	D6	Digital I/O 6 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD} = 1$ or $\overline{CS} = 1$.
33	33	33	D7	Digital I/O 7 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD} = 1$ or $\overline{CS} = 1$.
34	34	34	D8	Digital Output 8 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD} = 1$ or $\overline{CS} = 1$.
35	35	35	D9	Digital Output 9 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD} = 1$ or $\overline{CS} = 1$.
36	36	36	D10	Digital Output 10 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD} = 1$ or $\overline{CS} = 1$.
37	37	37	D11	Digital Output 11 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD} = 1$ or $\overline{CS} = 1$.
40	40	40	\overline{EOC}	End-of-Conversion Output. \overline{EOC} goes low to indicate the end of a conversion. It returns high on the next rising CLK edge or the falling CONVST edge.
41	41	41	\overline{EOLC}	End-of-Last-Conversion Output. \overline{EOLC} goes low to indicate the end of the last conversion. It returns high when CONVST goes low for the next conversion sequence.
42	42	42	\overline{RD}	Read Input. Pulling \overline{RD} low initiates a read command of the parallel data bus.
43	43	43	\overline{WR}	Write Input. Pulling \overline{WR} low initiates a write command for configuring the device with D0–D7.

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10V$, $\pm 5V$, and 0 to +5V Analog Input Ranges

Pin Description (continued)

PIN			NAME	FUNCTION
MAX1304 MAX1308 MAX1312	MAX1305 MAX1309 MAX1313	MAX1306 MAX1310 MAX1314		
44	44	44	\overline{CS}	Chip-Select Input. Pulling \overline{CS} low activates the digital interface. Forcing \overline{CS} high places D0–D11 in high-impedance mode.
45	45	45	CONVST	Conversion Start Input. Driving CONVST high initiates the conversion process. The analog inputs are sampled on the rising edge of CONVST.
46	46	46	CLK	External Clock Input. For external clock operation, connect INTCLK/ \overline{EXTCLK} to DGND and drive CLK with an external clock signal from 100kHz to 20MHz. For internal clock operation, connect INTCLK/ \overline{EXTCLK} to DV _{DD} and connect CLK to DGND.
47	47	47	SHDN	Shutdown Input. Driving SHDN high initiates device shutdown. Connect SHDN to DGND for normal operation.
48	48	48	\overline{CHSHDN}	Active-Low Analog-Input Channel-Shutdown Input. Drive \overline{CHSHDN} low to power down analog inputs that are not selected for conversion in the configuration register. Drive \overline{CHSHDN} high to power up all analog input channels regardless of whether they are selected for conversion in the configuration register. See the <i>Channel Shutdown (\overline{CHSHDN})</i> section for more information.
—	9, 10, 11, 12	7, 8, 9, 10, 11, 12	I.C.	Internally connected. Connect I.C. to AGND.

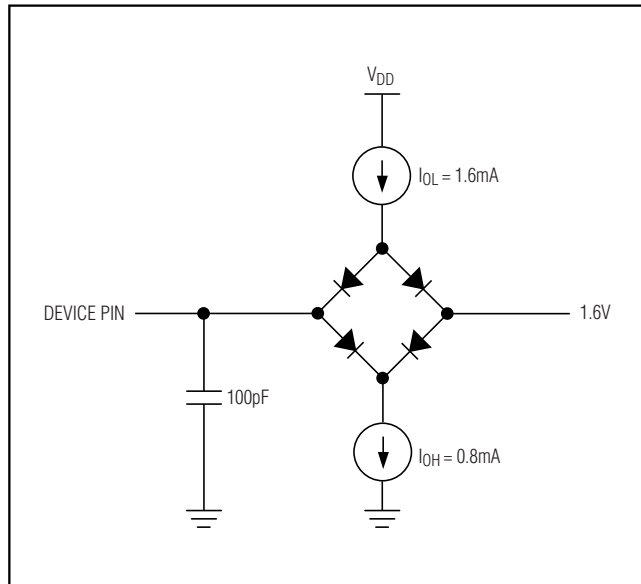


Figure 1. Digital Load Test Circuit

Detailed Description

The MAX1304–MAX1306/MAX1308–MAX1310/MAX1312–MAX1314 are 12-bit ADCs. The devices offer 8, 4, or 2 independently selectable input channels, each with dedicated T/H circuitry. Simultaneous sampling of all active channels preserves relative phase information making these devices ideal for motor control and power monitoring. Three input ranges are available, 0 to +5V, $\pm 5V$ and $\pm 10V$. The 0 to +5V devices provide $\pm 6V$ fault-tolerant inputs. The $\pm 5V$ and $\pm 10V$ devices provide $\pm 16.5V$ fault-tolerant inputs. Two-channel conversion results are available in 0.9 μs . Conversion results from all eight channels are available in 1.98 μs . The 8-channel throughput is 456ksps per channel. Internal or external reference and clock capability offer great flexibility, and ease of use. A write-only configuration register can mask out unused channels and a shutdown feature reduces power. A 20MHz, 12-bit, parallel data bus outputs the conversion results. Figure 2 shows the functional diagram of these ADCs.

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10V$, $\pm 5V$, and 0 to +5V Analog Input Ranges

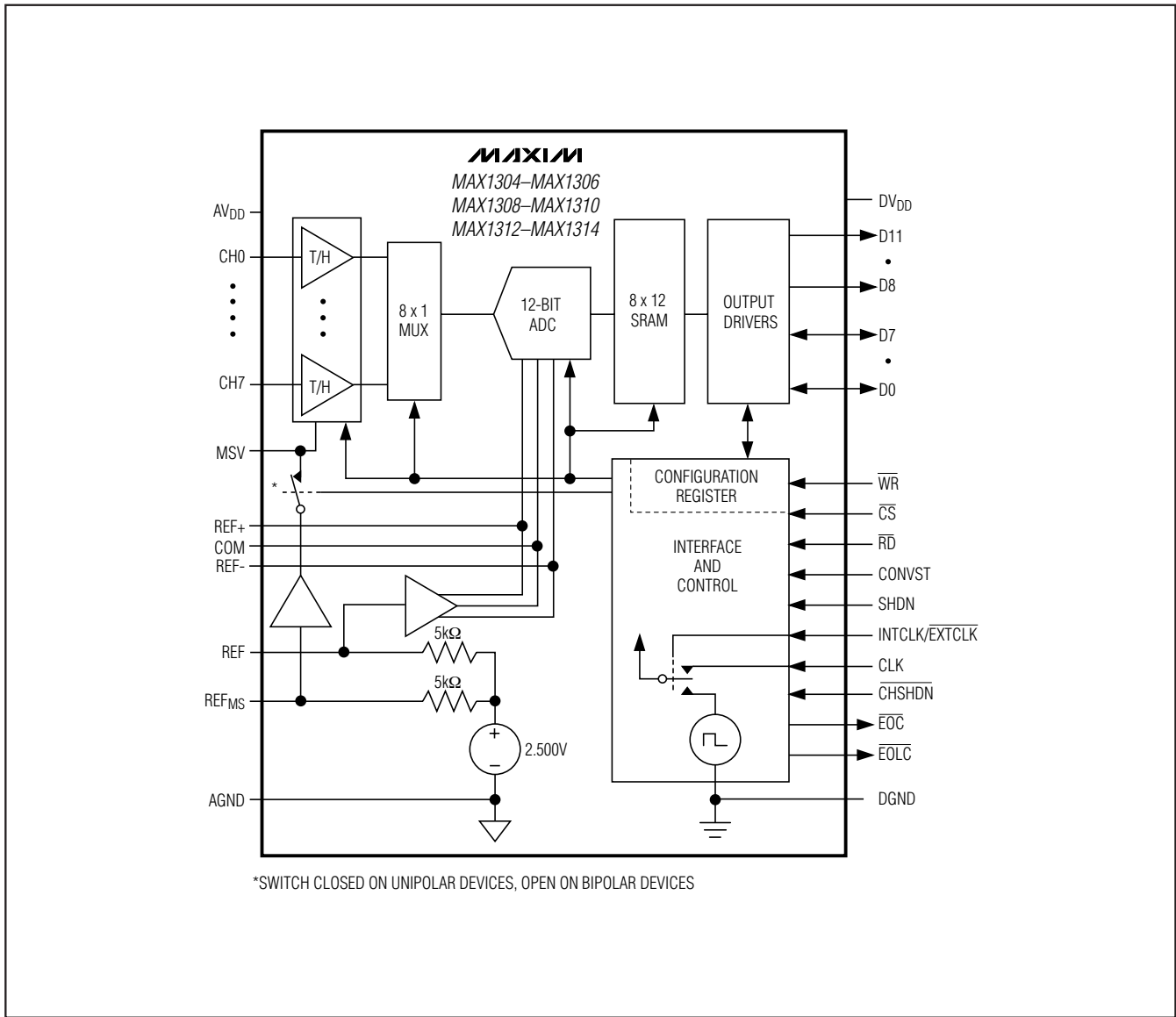


Figure 2. Functional Diagram

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

MAX1304-MAX1306/MAX1308-MAX1310/MAX1312-MAX1314

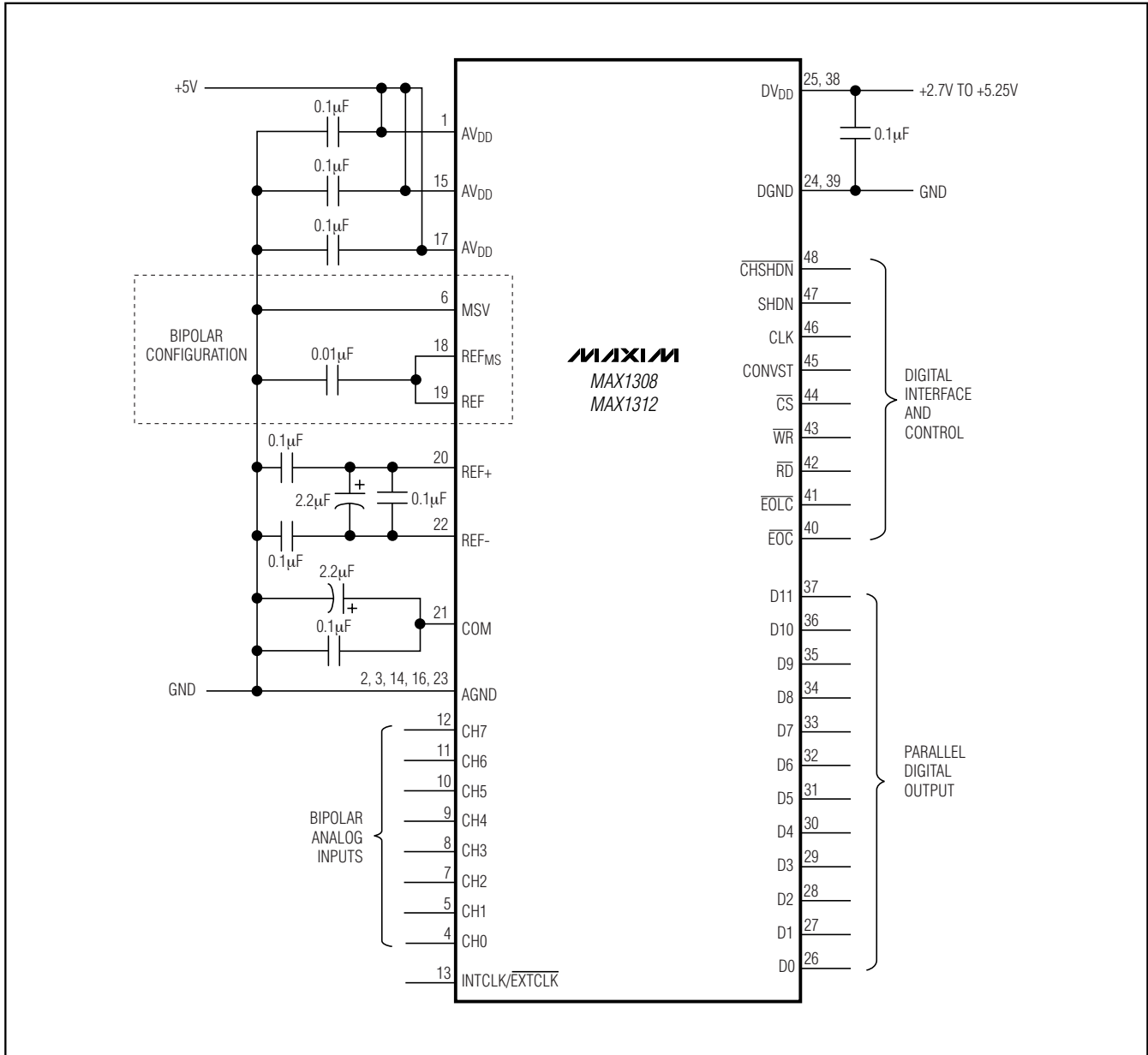


Figure 3. Typical Bipolar Operating Circuit

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

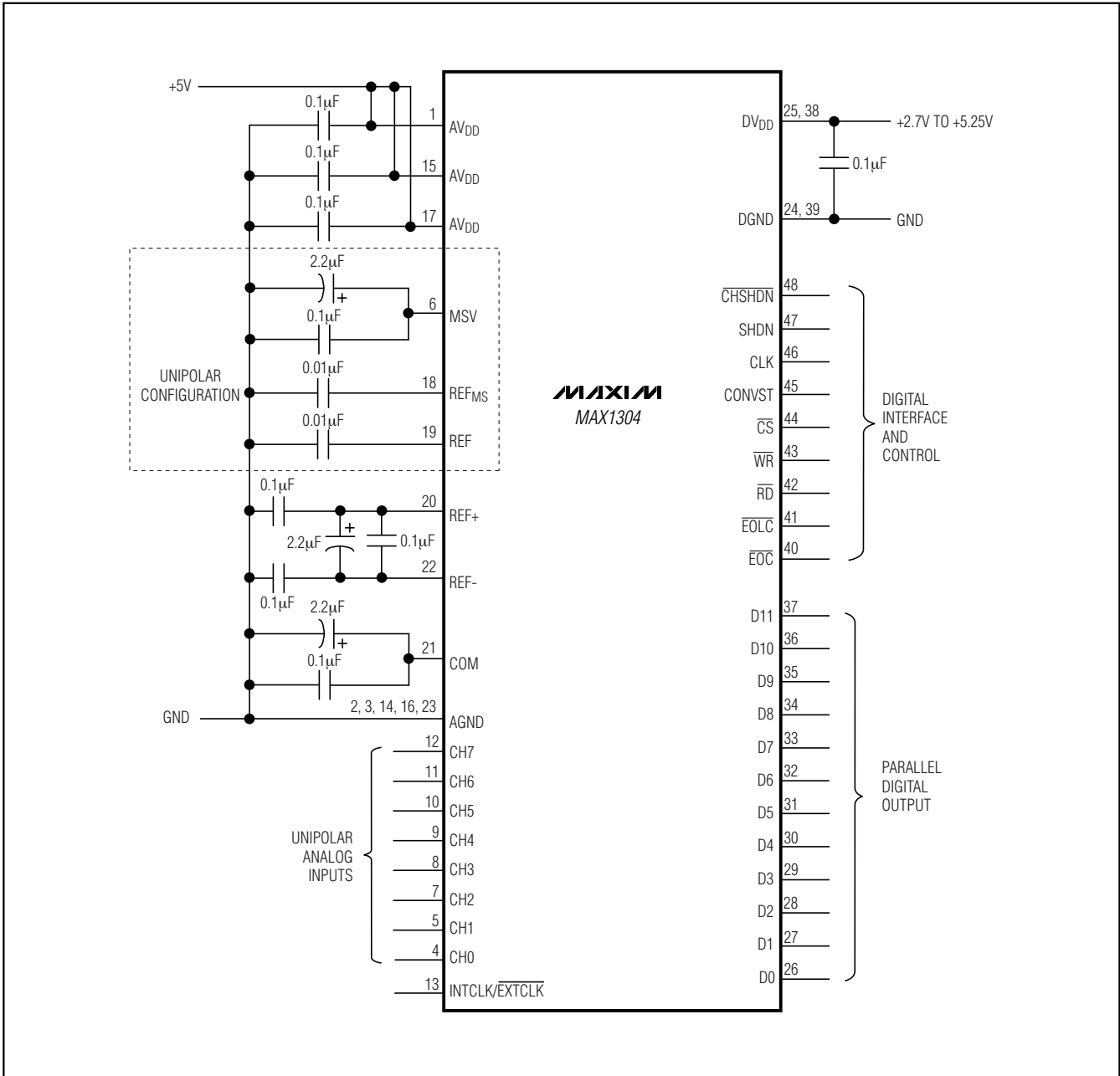


Figure 4. Typical Unipolar Operating Circuit

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

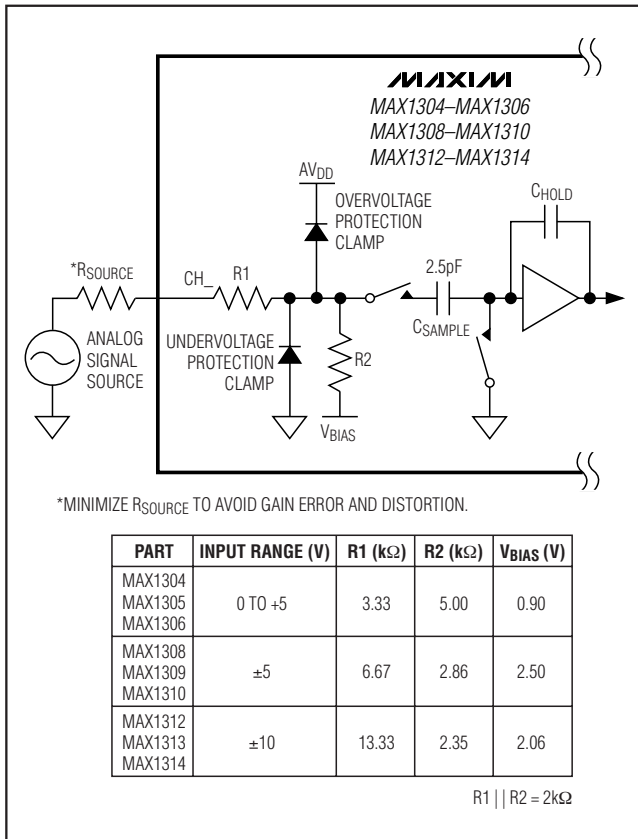


Figure 5. Single-Channel, Equivalent Analog Input T/H Circuit

Analog Inputs

Track and Hold (T/H)

To preserve phase information across the multichannel MAX1304–MAX1306/MAX1308–MAX1310/MAX1312–MAX1314, all input channels have dedicated T/H amplifiers. Figure 5 shows the equivalent analog input T/H circuit for one channel.

The input T/H circuit is controlled by the CONVST input. When CONVST is low, the T/H circuit tracks the analog input. When CONVST is high the T/H circuit holds the analog input. The rising edge of CONVST is the analog input sampling instant. There is an aperture delay (t_{AD}) of 8ns and a 50psRMS aperture jitter (t_{AJ}). The aperture delay of each dedicated T/H input is matched within 100ps of each other.

To settle the charge on C_{SAMPLE} to 12-bit accuracy, use a minimum acquisition time (t_{ACQ}) of 100ns. Therefore, CONVST must be low for at least 100ns. Although longer acquisition times allow the analog input to settle to its final value more accurately, the maximum

acquisition time must be limited to 1ms. Accuracy with conversion times longer than 1ms cannot be guaranteed due to capacitor droop in the input circuitry.

Due to the analog input resistive divider formed by R1 and R2 in Figure 5, any significant analog input source resistance (R_{SOURCE}) results in gain error. Furthermore, R_{SOURCE} causes distortion due to nonlinear analog input currents. Limit R_{SOURCE} to a maximum of 100Ω.

Selecting an Input Buffer

To improve the input signal bandwidth under AC conditions, drive the input with a wideband buffer (>50MHz) that can drive the ADC's input capacitance (15pF) and settle quickly. For example, the MAX4431 or the MAX4265 can be used for the 0 to +5V unipolar devices, or the MAX4350 can be used for ±5V bipolar inputs.

Most applications require an input buffer to achieve 12-bit accuracy. Although slew rate and bandwidth are important, the most critical input buffer specification is settling time. The simultaneous sampling of multiple channels requires an acquisition time of 100ns. At the beginning of the acquisition, the ADC internal sampling capacitor array connects to the analog inputs, causing some disturbance. Ensure the amplifier is capable of settling to at least 12-bit accuracy during this interval. Use a low-noise, low-distortion, wideband amplifier that settles quickly and is stable with the ADC's 15pF input capacitance.

See the Maxim website at www.maxim-ic.com for application notes on how to choose the optimum buffer amplifier for your ADC application.

Input Bandwidth

The input-tracking circuitry has a 20MHz small-signal bandwidth, making it possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Input Range and Protection

The MAX1304/MAX1305/MAX1306 provide a 0 to +5V input voltage range with fault protection of ±6V. The MAX1308/MAX1309/MAX1310 provide a ±5V input voltage range with fault protection of ±16.5V. The MAX1312/MAX1313/MAX1314 provide a ±10V input voltage range with fault protection of ±16.5V. Figure 5 shows the single-channel equivalent input circuit.

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

Data Throughput

The data throughput (f_{TH}) of the MAX1304–MAX1306/MAX1308–MAX1310/MAX1312–MAX1314 is a function of the clock speed (f_{CLK}). In internal clock mode, $f_{CLK} = 15\text{MHz}$ (typ). In external clock mode, $100\text{kHz} \leq f_{CLK} \leq 20\text{MHz}$. When reading during conversion (Figures 7 and 8), calculate f_{TH} as follows:

$$f_{TH} = \frac{1}{t_{ACQ} + t_{QUIET} + \frac{12 + 3 \times (N-1) + 1}{f_{CLK}}}$$

where N is the number of active channels and t_{QUIET} is the period of bus inactivity before the rising edge of CONVST. See the *Starting a Conversion* section for more information.

Table 1 uses the above equation and shows the total throughput as a function of the number of channels selected for conversion.

Clock Modes

The MAX1304–MAX1306/MAX1308–MAX1310/MAX1312–MAX1314 provide a 15MHz internal conversion clock. Alternatively, an external clock can be used.

Internal Clock

Internal clock mode frees the microprocessor from the burden of running the ADC conversion clock. For internal clock operation, connect INTCLK/EXTCLK to AV_{DD} and connect CLK to DGND. Note that INTCLK/EXTCLK is referenced to AV_{DD}, not DV_{DD}.

External Clock

For external clock operation, connect INTCLK/EXTCLK to AGND and connect an external clock source to CLK. Note that INTCLK/EXTCLK is referenced to AV_{DD}, not DV_{DD}. The external clock frequency can be up to 20MHz. Linearity is not guaranteed with clock frequencies below 100kHz due to droop in the T/H circuits.

Table 1. Throughput vs. Channels Sampled: $f_{CLK} = 15\text{MHz}$, $t_{ACQ} = 100\text{ns}$, $t_{QUIET} = 50\text{ns}$

CHANNELS SAMPLED (N)	CLOCK CYCLES UNTIL LAST RESULT	CLOCK CYCLE FOR READING LAST CONVERSION	TOTAL CONVERSION TIME (ns)	TOTAL THROUGHPUT (ksps)	THROUGHPUT PER CHANNEL (f_{TH})
1	12	1	800	983	983
2	15	1	1000	1643	821
3	18	1	1200	2117	705
4	21	1	1400	2474	618
5	24	1	1600	2752	550
6	27	1	1800	2975	495
7	30	1	2000	3157	451
8	33	1	2200	3310	413

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

Applications Information

Digital Interface

The bidirectional parallel digital interface allows for setting the 8-bit configuration register (see the *Configuration Register* section) and reading the 12-bit conversion result. The interface includes the following control signals: chip select (\overline{CS}), read (\overline{RD}), write (\overline{WR}), end of conversion (\overline{EOC}), end of last conversion (\overline{EOLC}), conversion start (\overline{CONVST}), shutdown (\overline{SHDN}), channel shutdown (\overline{CHSHDN}), internal clock select ($\overline{INTCLK/EXTCLK}$), and external clock input (\overline{CLK}). Figures 6, 7, 8, 9, Table 2, and the *Timing Characteristics* show the operation of the interface. D0–D7 are bidirectional, and D8–D11 are output only. D0–D11 go high impedance when $\overline{RD} = 1$ or $\overline{CS} = 1$.

Configuration Register

Enable channels as active by writing to the configuration register through I/O lines D0–D7 (Table 2). The bits in the configuration register map directly to the channels, with D0 controlling channel zero, and D7 controlling channel seven. Setting any bit high activates the corresponding input channel, while resetting any bit low deactivates the corresponding channel. On the devices with less than eight channels, some of the bits have no function (Table 2).

To write to the configuration register, pull \overline{CS} and \overline{WR} low, load bits D0 through D7 onto the parallel bus, and force \overline{WR} high. The data are latched on the rising edge of \overline{WR} (Figure 6). Write to the configuration register at any point during the conversion sequence. At power-up, write to the configuration register to select the active channels before beginning a conversion.

However, the new configuration does not take effect until the next \overline{CONVST} falling edge. At power-up all channels default active. Shutdown does not change the configuration register. The configuration register may be written to in shutdown. See the *Channel Shutdown* (\overline{CHSHDN}) section for information about using the configuration register for power saving.

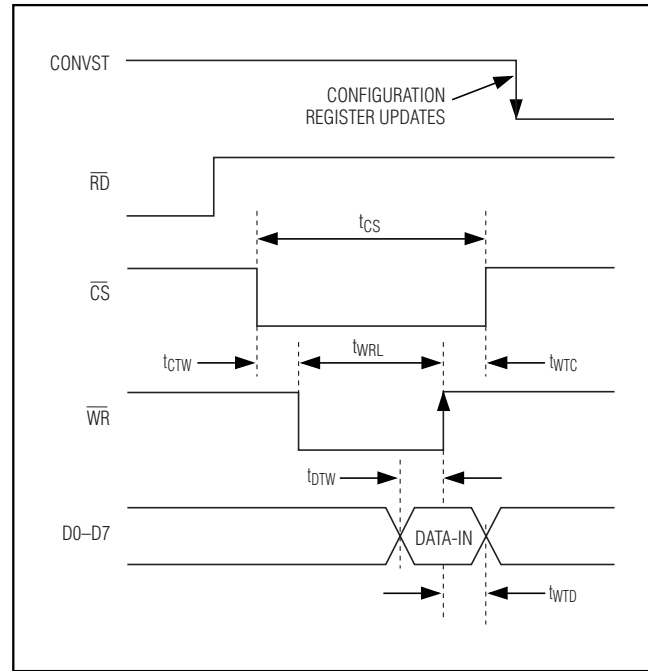


Figure 6. Write Timing

Table 2. Configuration Register

PART NUMBER	STATE	BIT/CHANNEL							
		D0/CH0	D1/CH1	D2/CH2	D3/CH3	D4/CH4	D5/CH5	D6/CH6	D7/CH7
MAX1304 MAX1308 MAX1312	ON	1	1	1	1	1	1	1	1
	OFF	0	0	0	0	0	0	0	0
MAX1305 MAX1309 MAX1313	ON	1	1	1	1	X	X	X	X
	OFF	0	0	0	0	X	X	X	X
MAX1306 MAX1310 MAX1314	ON	1	1	X	X	X	X	X	X
	OFF	0	0	X	X	X	X	X	X

X = Don't care (must be 1 or 0).

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

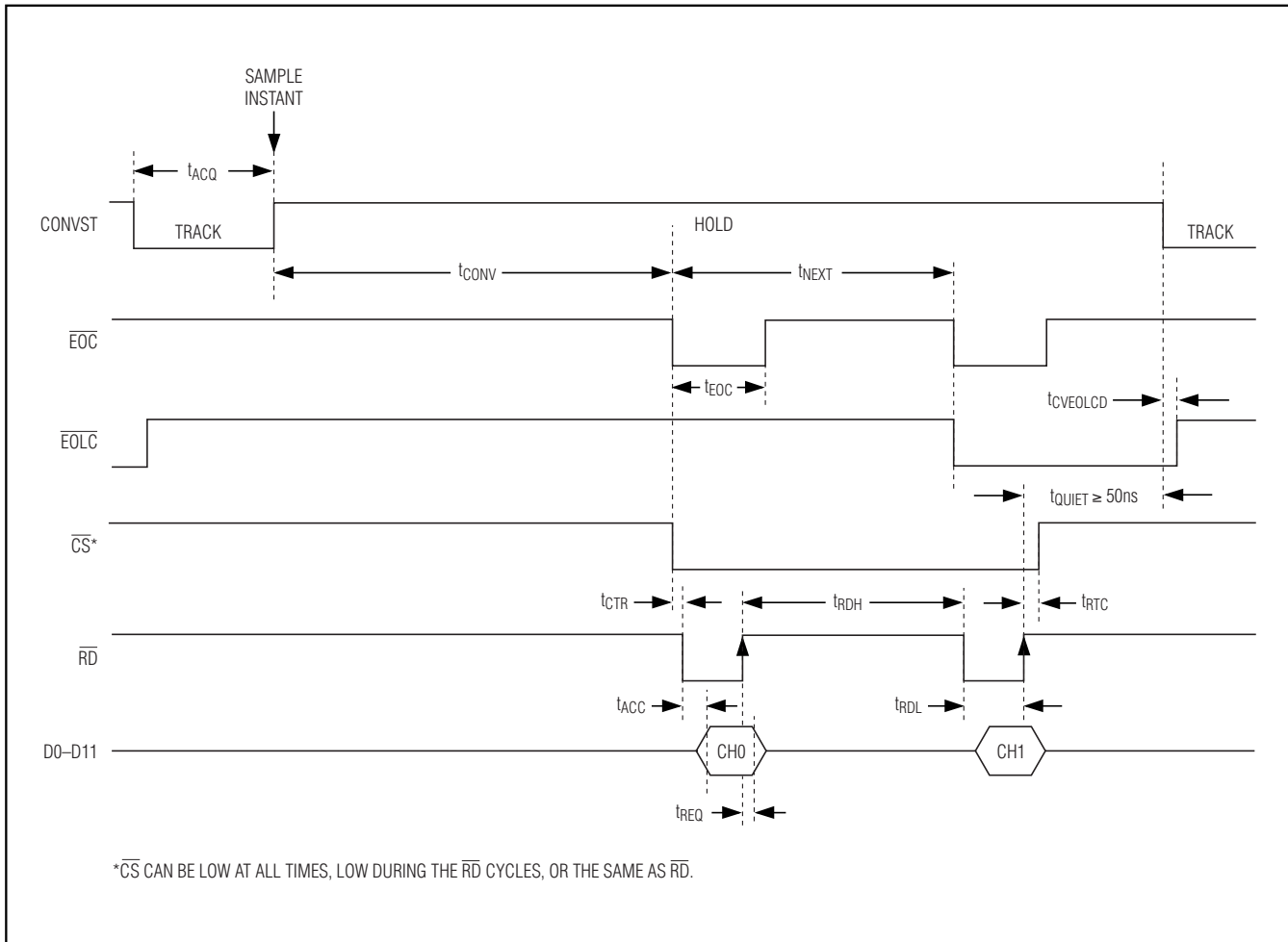


Figure 7. Read During Conversion—Channel 0 and Channel 1 Selected, Internal Clock

Starting a Conversion

To start a conversion using internal clock mode, pull CONVST low for the acquisition time (t_{ACQ}). The T/H acquires the signal while CONVST is low, and conversion begins on the rising edge of CONVST. The end-of-conversion signal (\overline{EOC}) pulses low whenever a conversion result becomes available for read. The end-of-last-conversion signal (\overline{EOLC}) goes low when the last conversion result is available (Figure 7).

To start a conversion using external clock mode, pull CONVST low for the acquisition time (t_{ACQ}). The T/H acquires the signal while CONVST is low. The rising edge of CONVST is the sampling instant. Apply an external clock to CLK to start the conversion. To avoid T/H droop degrading the sampled analog input signals,

the first CLK pulse must occur within 10 μ s from the rising edge of CONVST. Additionally, the external clock frequency must be greater than 100kHz to avoid T/H droop-degrading accuracy. The first conversion result is available for read when \overline{EOC} goes low on the rising edge of the 13th clock cycle. Subsequent conversion results are available after every third clock cycle thereafter (Figures 8 and 9).

In both internal and external clock modes, hold CONVST high until the last conversion result is read. If CONVST goes low in the middle of a conversion, the current conversion is aborted and a new conversion is initiated. Furthermore, there must be a period of bus inactivity (t_{QUIET}) for 50ns or longer before the falling edge of CONVST for the specified ADC performance.

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

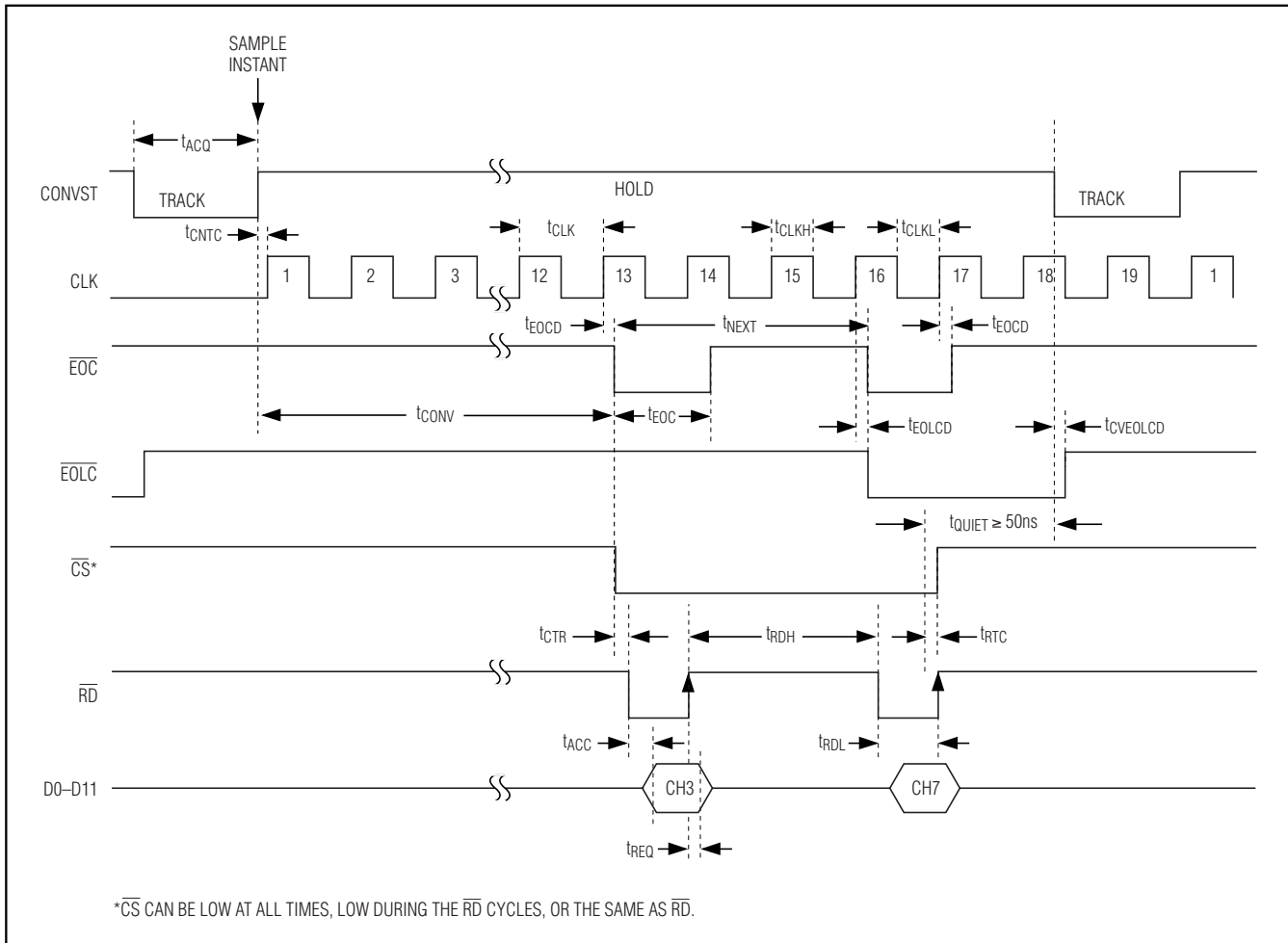


Figure 8. Read During Conversion—Channel 3 and Channel 7 Selected, External Clock

Reading a Conversion Result

Reading During a Conversion

Figures 7 and 8 show the interface signals to initiate a read operation during a conversion cycle. These figures show two channels selected for conversion. If more channels are selected, the results are available successively at every \overline{EOC} falling edge. \overline{CS} can be low at all times, low during the \overline{RD} cycles, or the same as \overline{RD} .

After initiating a conversion by bringing CONVST high, wait for \overline{EOC} to go low. In internal clock mode, \overline{EOC} goes low within 900ns. In external clock mode, \overline{EOC} goes low on the rising edge of the 13th CLK cycle. To read the conversion result, drive \overline{CS} and \overline{RD} low to latch data to the parallel digital output bus. Bring \overline{RD}

high to release the digital bus. In internal clock mode, the next \overline{EOC} falling edge occurs within 225ns. In external clock mode, the next \overline{EOC} falling edge occurs in three CLK cycles. When the last result is available \overline{EOLC} goes low.

Reading After Conversion

Figure 9 shows the interface signals for a read operation after a conversion with all eight channels enabled. At the falling of \overline{EOLC} , driving \overline{CS} and \overline{RD} low places the first conversion result onto the parallel bus. Successive low pulses of \overline{RD} place the successive conversion results onto the bus. When the last conversion results in the sequence are read, additional read pulses wrap the pointer back to the first converted result.

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10V$, $\pm 5V$, and 0 to +5V Analog Input Ranges

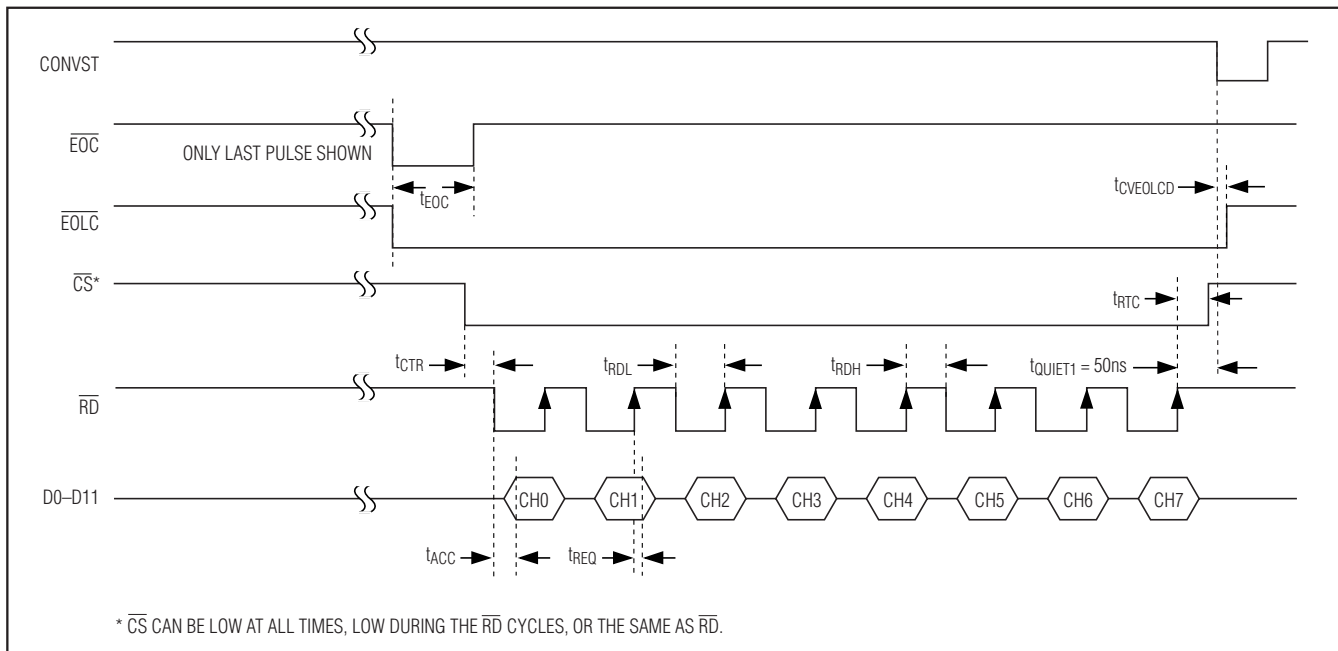


Figure 9. Read After Conversion—Eight Channels Selected, External Clock

Power-Up Reset

At power-up, all channels are selected for conversion (see the *Configuration Register* section). After applying power, allow the 1ms wake-up time to elapse and then initiate a dummy conversion and discard the results. After the dummy conversion is complete, accurate conversions can be obtained.

Power-Saving Modes

Shutdown Mode

During shutdown the internal reference and analog circuits in the device shutdown and the analog supply current drops to 0.6 μ A (typ). Select shutdown mode using the SHDN input. Set SHDN high to enter shutdown mode. SHDN takes precedence over CHSHDN.

Entering and exiting shutdown mode does not change the configuration byte. However, a new configuration byte can be written while in shutdown mode by following the standard write procedure shown in Figure 6.

\overline{EOC} and \overline{EOLC} are high when the MAX1304-MAX1306/MAX1308-MAX1310/MAX1312-MAX1314 are shut down.

The state of the digital outputs D0-D11 is independent of the state of SHDN. If \overline{CS} and \overline{RD} are low, the digital outputs D0-D11 are active regardless of SHDN. The digital outputs only go high impedance when \overline{CS} or \overline{RD} is high. When the digital outputs are powered down, the digital supply current drops to 20nA.

Exiting shutdown (falling edge of SHDN) starts a conversion in the same way as the rising edge of CONVST. After coming out of shutdown, initiate a dummy conversion and discard the results. After the dummy conversion, allow the 1ms wake-up time to expire before initiating the first accurate conversion.

Channel Shutdown (\overline{CHSHDN})

The channel-shutdown feature allows analog input channels to be powered down when they are not selected for conversion. Powering down channels that are not selected for conversion reduces the analog supply current by 2.9mA per channel. To power down channels that are not selected for conversion, pull \overline{CHSHDN} low. See the *Configuration Register* section for information on selecting and deselecting channels for conversion.

The drawback of powering down analog inputs that are not selected for conversion is that it takes time to power them up. Figure 10 shows how a dummy conversion is used to power up an analog input in external clock mode. After selecting a new channel in the configuration register, initiate a dummy conversion and discard the results. After the dummy conversion, allow the 1ms wake-up time (t_{WAKE}) to expire before initiating the first accurate conversion.

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

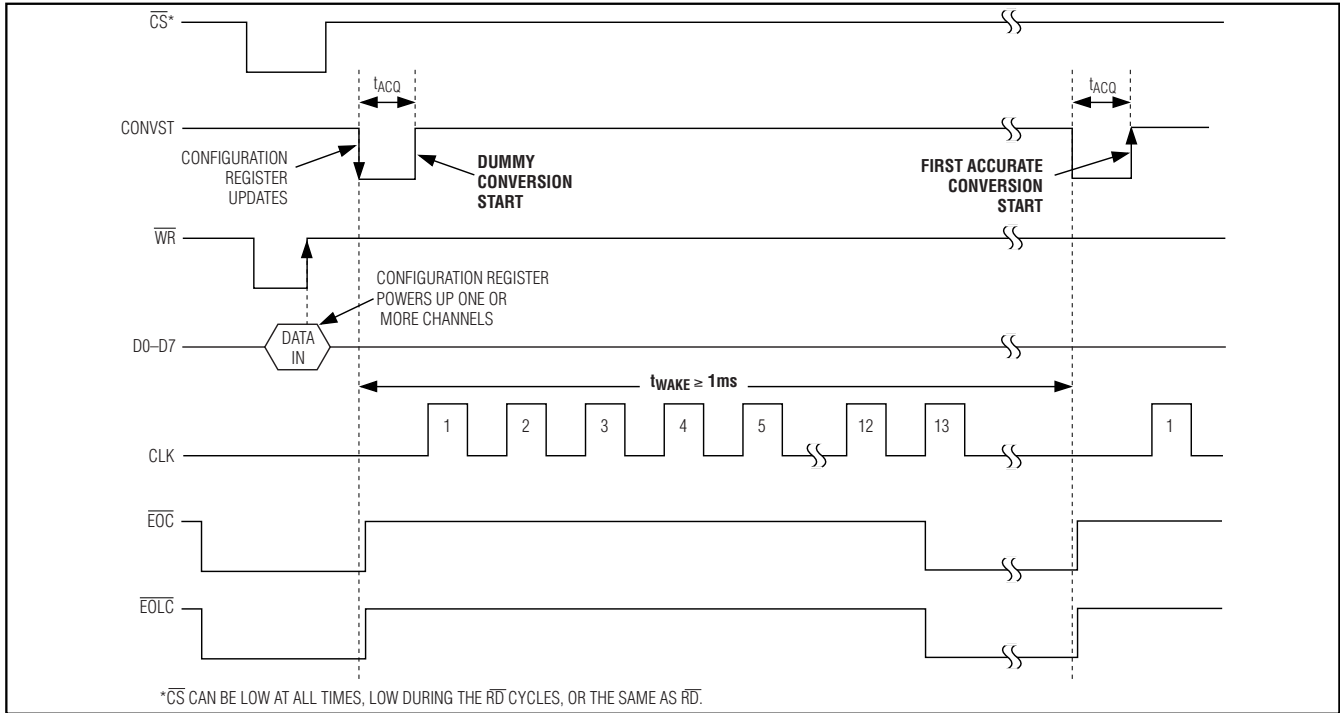


Figure 10. Powering Up an Analog Input Channel with a Dummy Conversion and Wake-Up Time ($\overline{CHSHDN} = 0$, External-Clock Mode, One Channel Selected)

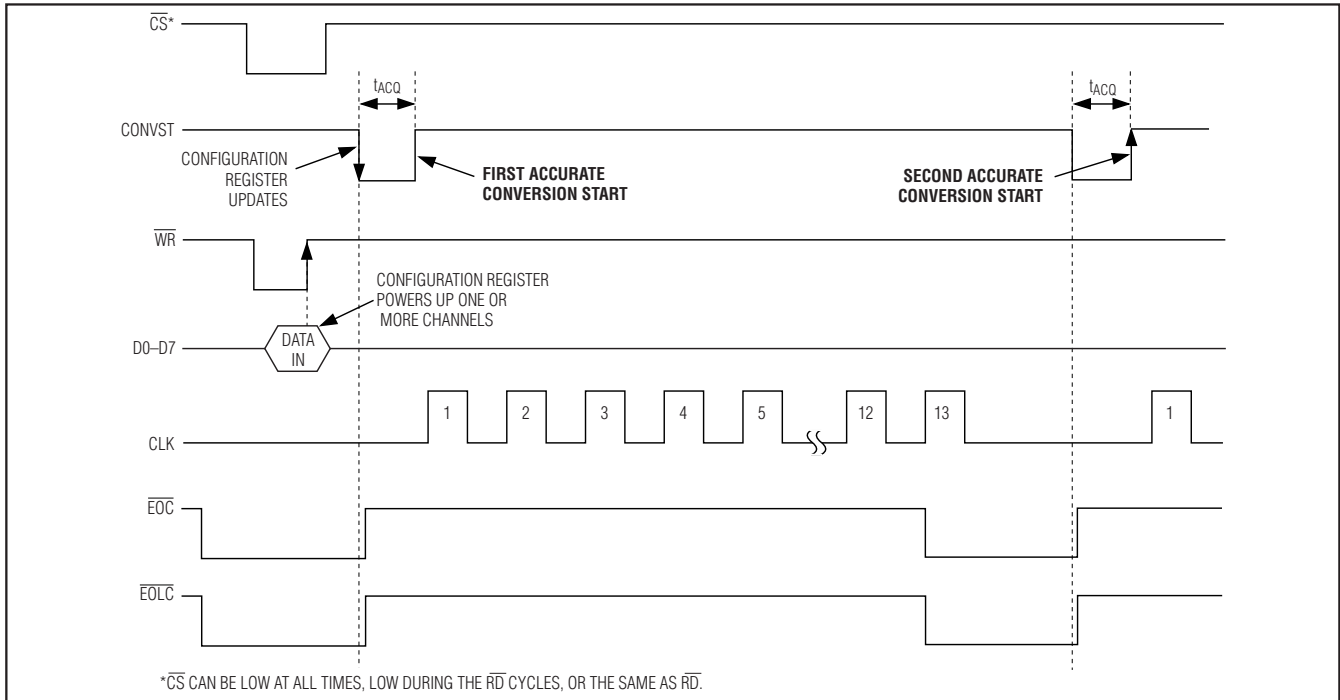


Figure 11. Powering Up an Analog Input Channel Directly ($\overline{CHSHDN} = 1$, External-Clock Mode, One Channel Selected)

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10\text{V}$, $\pm 5\text{V}$, and 0 to +5V Analog Input Ranges

To avoid the timing requirements associated with powering up an analog channel, force $\overline{\text{CHSHDN}}$ high. With $\overline{\text{CHSHDN}}$ high, each analog input is powered up regardless of whether it is selected for conversion in the configuration register. Note that shutdown mode takes precedence over the $\overline{\text{CHSHDN}}$ mode.

Reference

Internal Reference

The internal reference circuits provide for analog input voltages of 0 to +5V for the unipolar MAX1304/MAX1305/MAX1306, $\pm 5\text{V}$ for the bipolar MAX1308/MAX1309/MAX1310 or $\pm 10\text{V}$ for the bipolar MAX1312/MAX1313/MAX1314. Install external capacitors for reference stability, as indicated in Table 3 and shown in Figures 3 and 4.

As illustrated in Figure 2, the internal reference voltage is 2.5V (V_{REF}). This 2.5V is internally buffered to create the voltages at $\text{REF}+$ and $\text{REF}-$. Table 4 shows the voltages at COM, $\text{REF}+$, and $\text{REF}-$.

External Reference

External reference operation is achieved by overriding the internal reference voltage. Override the internal ref-

erence voltage by driving REF with a +2.0V to +3.0V external reference. As shown in Figure 2, the REF input impedance is $5\text{k}\Omega$. For more information about using external references see the *Transfer Functions* section.

Midscale Voltage (MSV)

The voltage at MSV (V_{MSV}) sets the midpoint of the ADC transfer functions. For the 0 to +5V input range (unipolar devices), the midpoint of the transfer function is +2.5V. For the $\pm 5\text{V}$ and $\pm 10\text{V}$ input range devices, the midpoint of the transfer function is zero.

As shown in Figure 2, there is a unity-gain buffer between REF_{MS} and MSV in the unipolar MAX1304/MAX1305/MAX1306. This midscale buffer sets the midpoint of the unipolar transfer functions to either the internal +2.5V reference or an externally applied voltage at REF_{MS} . V_{MSV} follows $V_{\text{REF}_{\text{MS}}}$ within $\pm 3\text{mV}$.

The midscale buffer is not active for the bipolar devices. For these devices, MSV must be connected to AGND or externally driven. REF_{MS} must be bypassed with a $0.01\mu\text{F}$ capacitor to AGND.

See the *Transfer Functions* section for more information about MSV.

Table 3. Reference Bypass Capacitors

LOCATION	INPUT VOLTAGE RANGE	
	UNIPOLAR (μF)	BIPOLAR (μF)
MSV Bypass Capacitor to AGND	2.2 0.1	N/A
REF_{MS} Bypass Capacitor to AGND	0.01	0.01
REF Bypass Capacitor to AGND	0.01	0.01
$\text{REF}+$ Bypass Capacitor to AGND	0.1	0.1
$\text{REF}+$ to $\text{REF}-$ Capacitor	2.2 0.1	2.2 0.1
$\text{REF}-$ Bypass Capacitor to AGND	0.1	0.1
COM Bypass Capacitor to AGND	2.2 0.1	2.2 0.1

N/A = Not applicable. Connect MSV directly to AGND.

Table 4. Reference Voltages

PARAMETER	EQUATION	CALCULATED VALUE (V) ($V_{\text{REF}} = 2.000\text{V}$, $AV_{\text{DD}} = 5.0\text{V}$)	CALCULATED VALUE (V) ($V_{\text{REF}} = 2.500\text{V}$, $AV_{\text{DD}} = 5.0\text{V}$)	CALCULATED VALUE (V) ($V_{\text{REF}} = 3.000\text{V}$, $AV_{\text{DD}} = 5.0\text{V}$)
V_{COM}	$V_{\text{COM}} = 13 / 25 \times AV_{\text{DD}}$	2.600	2.600	2.600
$V_{\text{REF}+}$	$V_{\text{REF}+} = V_{\text{COM}} + V_{\text{REF}} / 2$	3.600	3.850	4.100
$V_{\text{REF}-}$	$V_{\text{REF}-} = V_{\text{COM}} - V_{\text{REF}} / 2$	1.600	1.350	1.100
$V_{\text{REF}+} - V_{\text{REF}-}$	$V_{\text{REF}-} - V_{\text{REF}+} = V_{\text{REF}}$	2.000	2.500	3.000

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

Transfer Functions Unipolar 0 to +5V Devices

Table 5 and Figure 12 show the offset binary transfer function for the MAX1304/MAX1305/MAX1306 with a 0 to +5V input range. The full-scale input range (FSR) is two times the voltage at REF. The internal +2.5V reference gives a +5V FSR, while an external +2V to +3V reference allows an FSR of +4V to +6V, respectively. Calculate the LSB size using:

$$1 \text{ LSB} = \frac{2 \times V_{\text{REF}}}{2^{12}}$$

which equals 1.22mV when using a 2.5V reference.

The input range is centered about V_{MSV} , internally set to +2.5V. For a custom midscale voltage, drive REF_{MS} with an external voltage source and MSV will follow REF_{MS} . Noise present on MSV or REF_{MS} directly couples into the ADC result. Use a precision, low-drift voltage reference with adequate bypassing to prevent MSV from degrading ADC performance. For maximum FSR, do not violate the absolute maximum voltage ratings of the analog inputs when choosing MSV .

Determine the input voltage as a function of V_{REF} , V_{MSV} , and the output code in decimal using:

$$V_{\text{CH}_-} = \text{LSB} \times \text{CODE}_{10} + V_{\text{MSV}} - 2.500\text{V}$$

Table 5. 0 to 5V Unipolar Code Table

BINARY DIGITAL OUTPUT CODE	DECIMAL EQUIVALENT DIGITAL OUTPUT CODE (CODE ₁₀)	INPUT VOLTAGE (V) ($V_{\text{REF}} = +2.5\text{V}$) ($V_{\text{REFMS}} = +2.5\text{V}$)
1111 1111 1111 = 0xFFF	4095	+4.9994 ± 0.5 LSB
1111 1111 1110 = 0xFFE	4094	+4.9982 ± 0.5 LSB
1000 0000 0001 = 0x801	2049	+2.5018 ± 0.5 LSB
1000 0000 0000 = 0x800	2048	+2.5006 ± 0.5 LSB
0111 1111 1111 = 0x7FF	2047	+2.4994 ± 0.5 LSB
0000 0000 0001 = 0x001	1	+0.0018 ± 0.5 LSB
0000 0000 0000 = 0x000	0	+0.0006 ± 0.5 LSB

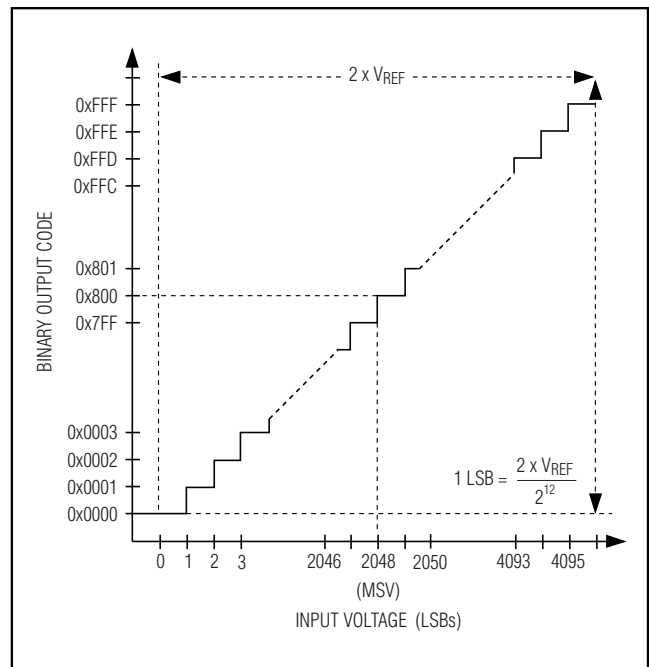


Figure 12. 0 to +5V Unipolar Transfer Function

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

Bipolar ±5V Devices

Table 6 and Figure 13 show the two's complement transfer function for the ±5V input range MAX1308/MAX1309/MAX1310. The FSR is four times the voltage at REF. The internal +2.5V reference gives a +10V FSR, while an external +2V to +3V reference allows an FSR of +8V to +12V respectively. Calculate the LSB size using:

$$1 \text{ LSB} = \frac{4 \times V_{REF}}{2^{12}}$$

which equals 2.44mV when using a 2.5V reference.

The input range is centered about V_{MSV} . Normally, $MSV = AGND$, and the input is symmetrical about zero. For a custom midscale voltage, drive MSV with an external voltage source. Noise present on MSV directly couples into the ADC result. Use a precision, low-drift voltage reference with adequate bypassing to prevent MSV from degrading ADC performance. For maximum FSR, do not violate the absolute maximum voltage ratings of the analog inputs when choosing MSV .

Determine the input voltage as a function of V_{REF} , V_{MSV} , and the output code in decimal using:

$$V_{CH_} = \text{LSB} \times \text{CODE}_{10} + V_{MSV}$$

Table 6. ±5V Bipolar Code Table

TWO'S COMPLEMENT DIGITAL OUTPUT CODE	DECIMAL EQUIVALENT DIGITAL OUTPUT CODE (CODE ₁₀)	INPUT VOLTAGE (V) ($V_{REF} = +2.5V$, $V_{MSV} = 0$)
0111 1111 1111 = 0x7FF	+2047	+4.9988 ± 0.5 LSB
0111 1111 1110 = 0x7FE	+2046	+4.9963 ± 0.5 LSB
0000 0000 0001 = 0x001	+1	+0.0037 ± 0.5 LSB
0000 0000 0000 = 0x000	0	+0.0012 ± 0.5 LSB
1111 1111 1111 = 0xFFF	-1	-0.0012 ± 0.5 LSB
1000 0000 0001 = 0x801	-2047	-4.9963 ± 0.5 LSB
1000 0000 0000 = 0x800	-2048	-4.9988 ± 0.5 LSB

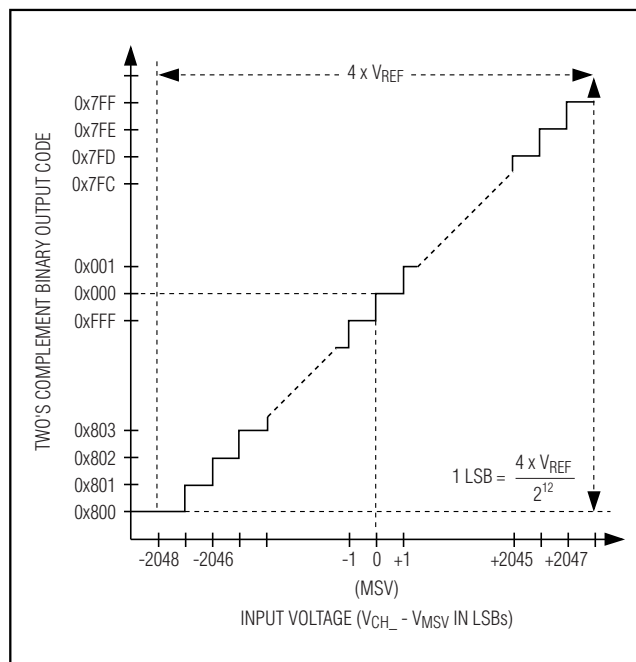


Figure 13. ±5V Bipolar Transfer Function

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

Bipolar ±10V Devices

Table 7 and Figure 14 show the two's complement transfer function for the ±10V input range MAX1312/MAX1313/MAX1314. The FSR is eight times the voltage at REF. The internal +2.5V reference gives a +20V FSR, while an external +2V to +3V reference allows an FSR of +16V to +24V, respectively. Calculate the LSB size using:

$$1 \text{ LSB} = \frac{8 \times V_{REF}}{2^{12}}$$

which equals 4.88mV with a +2.5V internal reference.

The input range is centered about V_{MSV} . Normally, $MSV = AGND$, and the input is symmetrical about zero. For a custom midscale voltage, drive MSV with an external voltage source. Noise present on MSV directly couples into the ADC result. Use a precision, low-drift voltage reference with adequate bypassing to prevent MSV from degrading ADC performance. For maximum FSR, do not violate the absolute maximum voltage ratings of the analog inputs when choosing MSV .

Determine the input voltage as a function of V_{REF} , V_{MSV} , and the output code in decimal using:

$$V_{CH_L} = \text{LSB} \times \text{CODE}_{10} + V_{MSV}$$

Table 7. ±10V Bipolar Code Table

TWO's COMPLEMENT DIGITAL OUTPUT CODE	DECIMAL EQUIVALENT DIGITAL OUTPUT CODE (CODE ₁₀)	INPUT VOLTAGE (V) ($V_{REF} = +2.5V$, $V_{MSV} = 0$)
0111 1111 1111 = 0x7FF	+2047	+9.9976 ± 0.5 LSB
0111 1111 1110 = 0x7FE	+2046	+9.9927 ± 0.5 LSB
0000 0000 0001 = 0x001	+1	+0.0073 ± 0.5 LSB
0000 0000 0000 = 0x000	0	0.0024 ± 0.5 LSB
1111 1111 1111 = 0xFFF	-1	-0.0024 ± 0.5 LSB
1000 0000 0001 = 0x801	-2047	-9.9927 ± 0.5 LSB
1000 0000 0000 = 0x800	-2048	-9.9976 ± 0.5 LSB

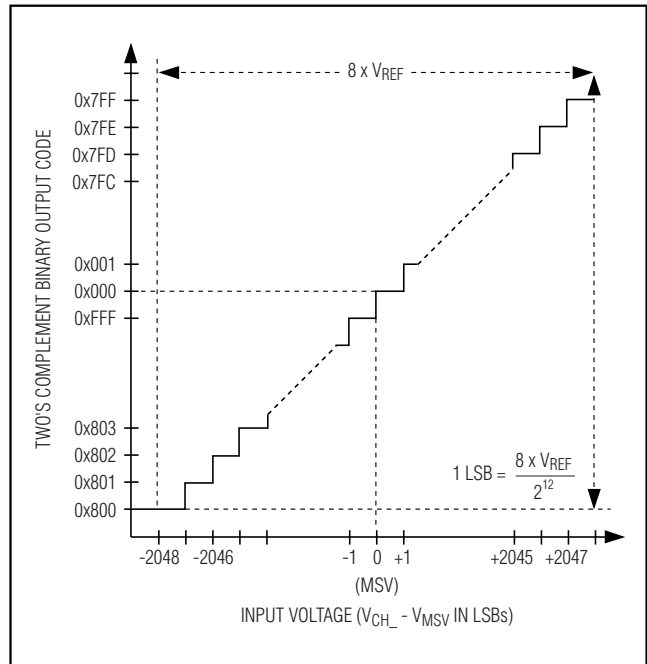


Figure 14. ±10V Bipolar Transfer Function

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

3-Phase Motor Controller

The MAX1304-MAX1306/MAX1308-MAX1310/MAX1312-MAX1314 are ideally suited for motor-control systems (Figure 15). The devices' simultaneously sampled inputs eliminate the need for complicated DSP algo-

rithms that realign sequentially sampled data into a simultaneous sample set. Additionally, the variety of input voltage ranges allows for flexibility when choosing current sensors and position encoders.

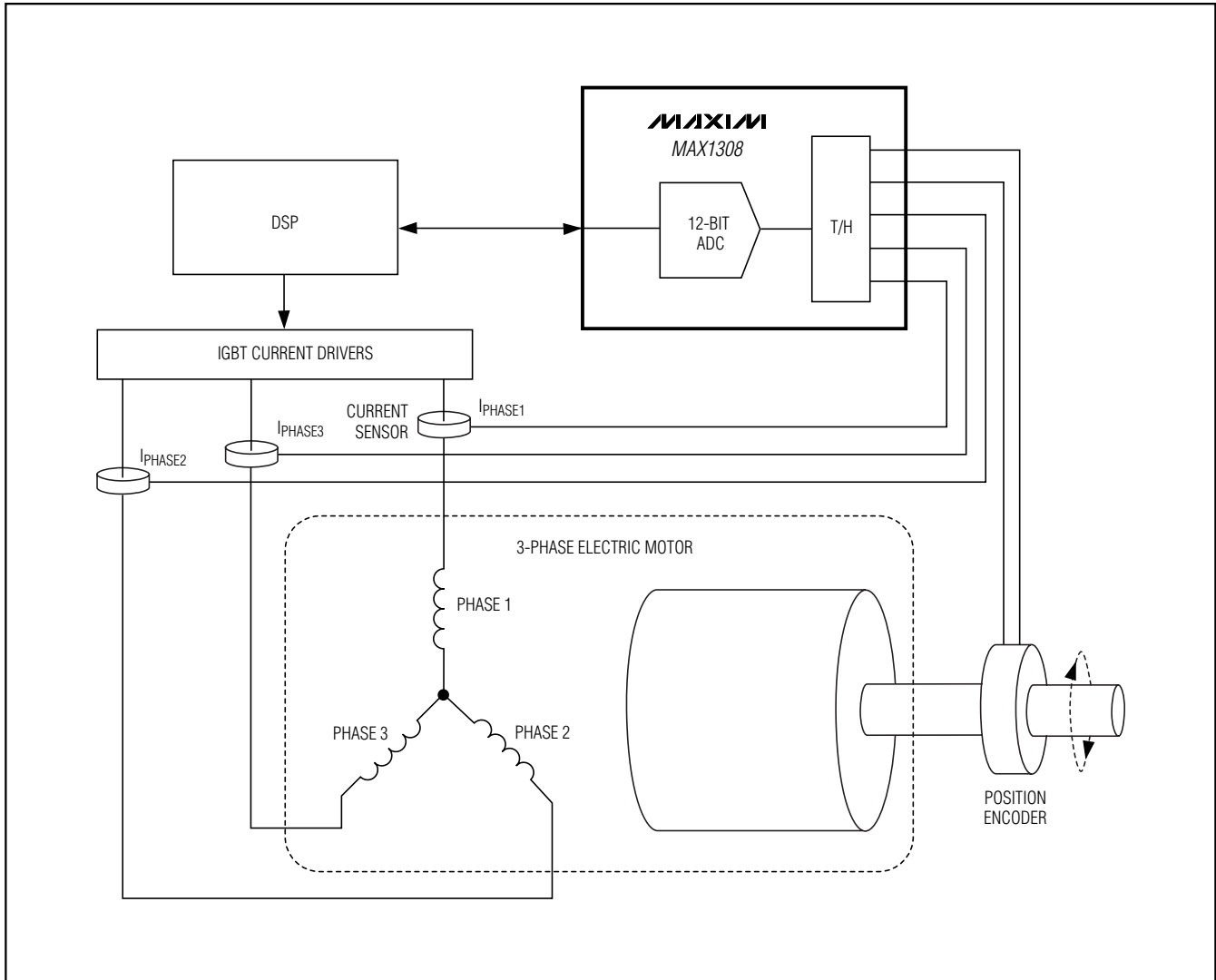


Figure 15. 3-Phase Motor Control

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10V$, $\pm 5V$, and 0 to +5V Analog Input Ranges

3-Phase Power-Monitoring System

The 8-channel devices are well suited for use in 3-phase power monitoring (Figure 16). The simultane-

ously sampled eight channels eliminate the need for complicated DSP algorithms that realign sequentially sampled data into a simultaneous sample set.

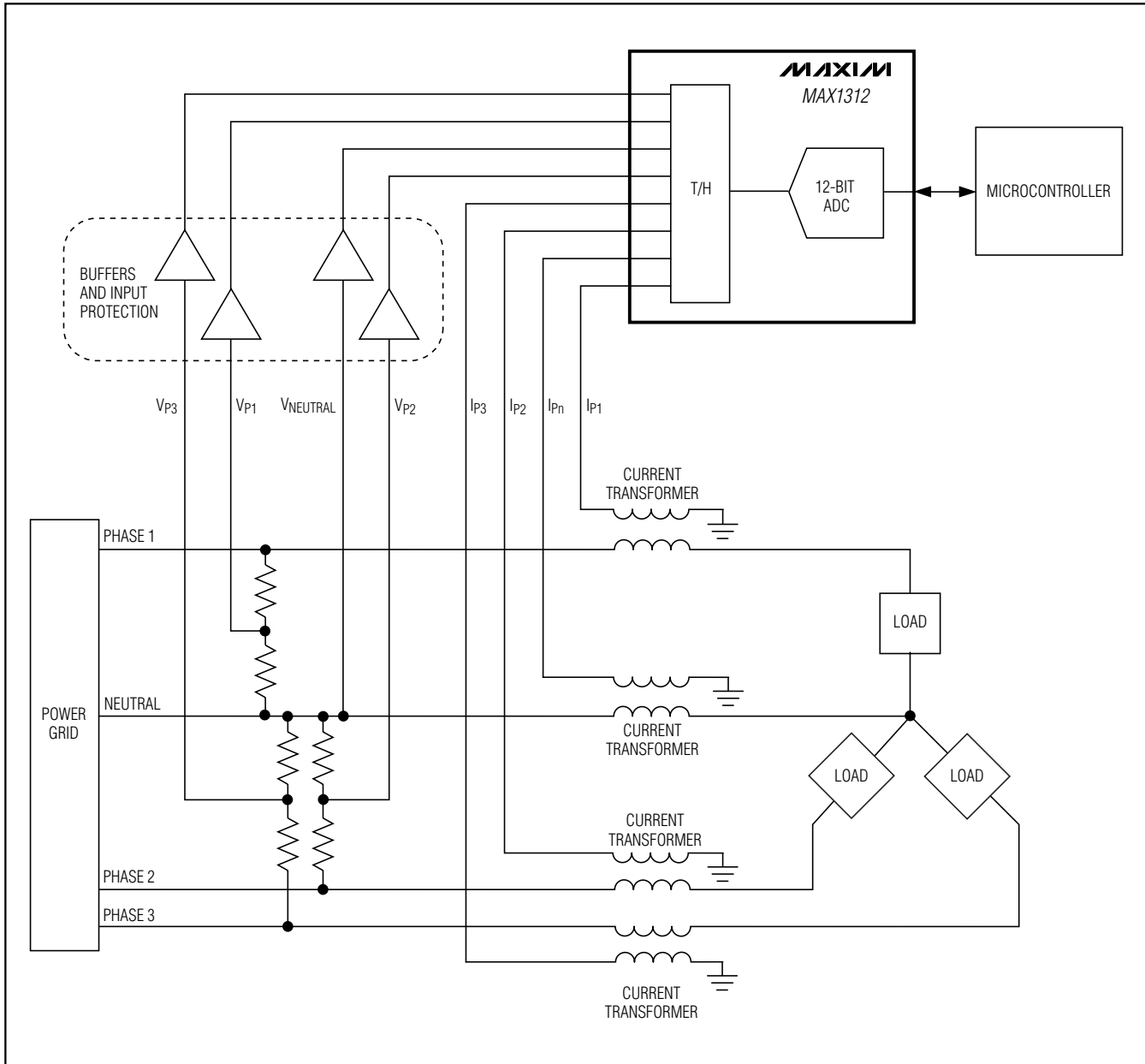


Figure 16. 3-Phase Power Monitoring

MAX1304-MAX1306-MAX1308-MAX1310-MAX1312-MAX1314

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10V$, $\pm 5V$, and 0 to +5V Analog Input Ranges

Layout, Grounding, and Bypassing

For best performance use PC boards. Board layout must ensure that digital and analog signal lines are separated from each other. Do not run analog and digital lines parallel to one another (especially clock lines), and do not run digital lines underneath the ADC package.

Figure 17 shows the recommended system ground connections. Establish an analog ground point at AGND and a digital ground point at DGND. Connect all analog grounds to the analog ground point. Connect all digital grounds to the digital ground point. For lowest noise operation, make the power-supply ground returns as low impedance and as short as possible. Connect the analog ground point to the digital ground point at one location.

High-frequency noise in the power supplies degrades the ADC's performance. Bypass the analog power plane to the analog ground plane with a 2.2 μF capacitor within one inch of the device. Bypass each AV_{DD} to AGND pair of pins with a 0.1 μF capacitor as close to the device as possible. AV_{DD} to AGND pairs are pin 1 to pin 2, pin 14 to pin 15, and pin 16 to pin 17. Likewise, bypass the digital power plane to the digital ground plane with a 2.2 μF capacitor within one inch of the device. Bypass each DV_{DD} to DGND pair of pins with a 0.1 μF capacitor as close to the device as possible. DV_{DD} to DGND pairs are pin 24 to pin 25, and pin 38 to pin 39. If a supply is very noisy use a ferrite bead as a lowpass filter as shown in Figure 17.

Definitions

Integral Nonlinearity (INL)

INL is the deviation of the values on an actual transfer function from a straight line. For these devices, this straight line is drawn between the endpoints of the transfer function, once offset and gain errors have been nullified.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step width and the ideal value of 1 LSB. For these devices, the DNL of each digital output code is measured and the worst-case value is reported in the electrical characteristics table. A DNL error specification of less than ± 1 LSB guarantees no missing codes and a monotonic transfer function.

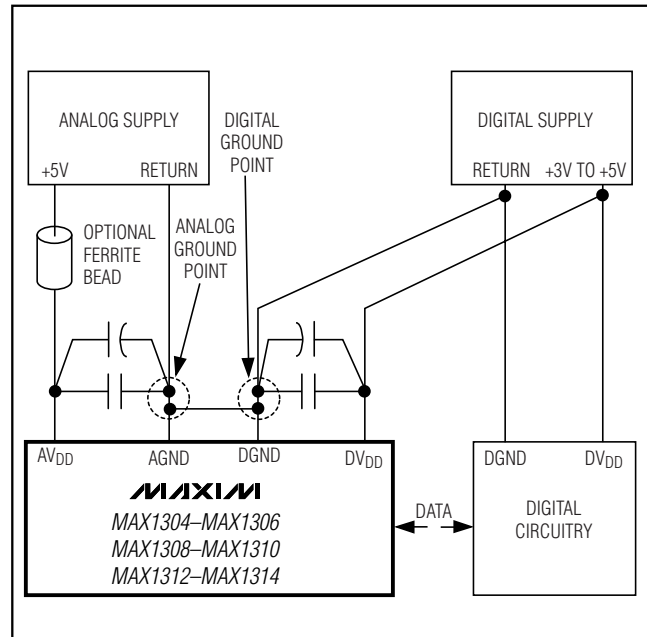


Figure 17. Power-Supply Grounding and Bypassing

Offset Error

Offset error is a figure of merit that indicates how well the actual transfer function matches the ideal transfer function at a single point. Typically the point at which offset error is specified is either at or near the zero-scale point of the transfer function or at or near the mid-scale point of the transfer function.

For the unipolar devices (MAX1304/MAX1305/MAX1306), the ideal zero-scale transition from 0x000 to 0x001 occurs at 1 LSB above AGND (Figure 12, Table 5). Unipolar offset error is the amount of deviation between the measured zero-scale transition point and the ideal zero-scale transition point.

For the bipolar devices (MAX1308/MAX1309/MAX1310/MAX1312/MAX1313/MAX1314), the ideal midscale transition from 0xFF to 0x000 occurs at MSV (Figures 14 and 13, Tables 7 and 6). The bipolar offset error is the amount of deviation between the measured midscale transition point and the ideal midscale transition point.

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10V$, $\pm 5V$, and 0 to +5V Analog Input Ranges

Gain Error

Gain error is a figure of merit that indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. For the MAX1304-MAX1306/MAX1308-MAX1310/MAX1312-MAX1314, the gain error is the difference of the measured full-scale and zero-scale transition points minus the difference of the ideal full-scale and zero-scale transition points.

For the unipolar devices (MAX1304/MAX1305/MAX1306), the full-scale transition point is from 0xFFE to 0xFFF and the zero-scale transition point is from 0x000 to 0x001.

For the bipolar devices (MAX1308/MAX1309/MAX1310/MAX1312/MAX1313/MAX1314), the full-scale transition point is from 0x7FE to 0x7FF and the zero-scale transition point is from 0x800 to 0x801.

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$\text{SNR}_{\text{dB}[\text{max}]} = 6.02\text{dB} \times N + 1.76\text{dB}$$

In reality, there are other noise sources such as thermal noise, reference noise, and clock jitter.

For these devices, SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency excluding the fundamental and the DC offset.

$$\text{SINAD}(\text{dB}) = 20 \times \log \left(\frac{\text{SIGNAL}_{\text{RMS}}}{(\text{NOISE} + \text{DISTORTION})_{\text{RMS}}} \right)$$

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed as:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}$$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first five harmonics to the fundamental itself. This is expressed as:

$$\text{THD} = 20 \times \log \left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1} \right)$$

where V_1 is the fundamental amplitude, and V_2 through V_6 are the amplitudes of the 2nd- through 6th-order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset. SFDR is specified in decibels relative to the carrier (dBc).

Channel-to-Channel Isolation

Channel-to-channel isolation indicates how well each analog input is isolated from the others. The channel-to-channel isolation for these devices is measured by applying DC to channel 1 through channel 7 while an AC 500kHz, -0.4dBFS sine wave is applied to channel 0. An FFT is taken for channel 0 and channel 1 and the difference (in dB) of the 500kHz magnitudes is reported as the channel-to-channel isolation.

Aperture Delay

Aperture delay (t_{AD}) is the time delay from the CONVST rising edge to the instant when an actual sample is taken.

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10V$, $\pm 5V$, and 0 to +5V Analog Input Ranges

Aperture Jitter

Aperture Jitter (t_{AJ}) is the sample-to-sample variation in aperture delay.

Jitter is a concern when considering an ADC's dynamic performance, e.g., SNR. To reconstruct an analog input from the ADC digital outputs, it is critical to know the time at which each sample was taken. Typical applications use an accurate sampling clock signal that has low jitter from sampling edge to sampling edge. For a system with a perfect sampling clock signal, with no clock jitter, the SNR performance of an ADC is limited by the ADC's internal aperture jitter as follows:

$$\text{SNR} = 20 \times \log \left(\frac{1}{2 \times \pi \times f_{IN} \times t_{AJ}} \right)$$

where f_{IN} represents the analog input frequency and t_{AJ} is the time of the aperture jitter.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC so that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB.

Full-Power Bandwidth

A large, -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB. This point is defined as full-power input bandwidth frequency.

DC Power-Supply Rejection (PSRR)

DC PSRR is defined as the change in the positive full-scale transfer function point caused by a $\pm 5\%$ variation in the analog power-supply voltage (A_{VDD}).

Chip Information

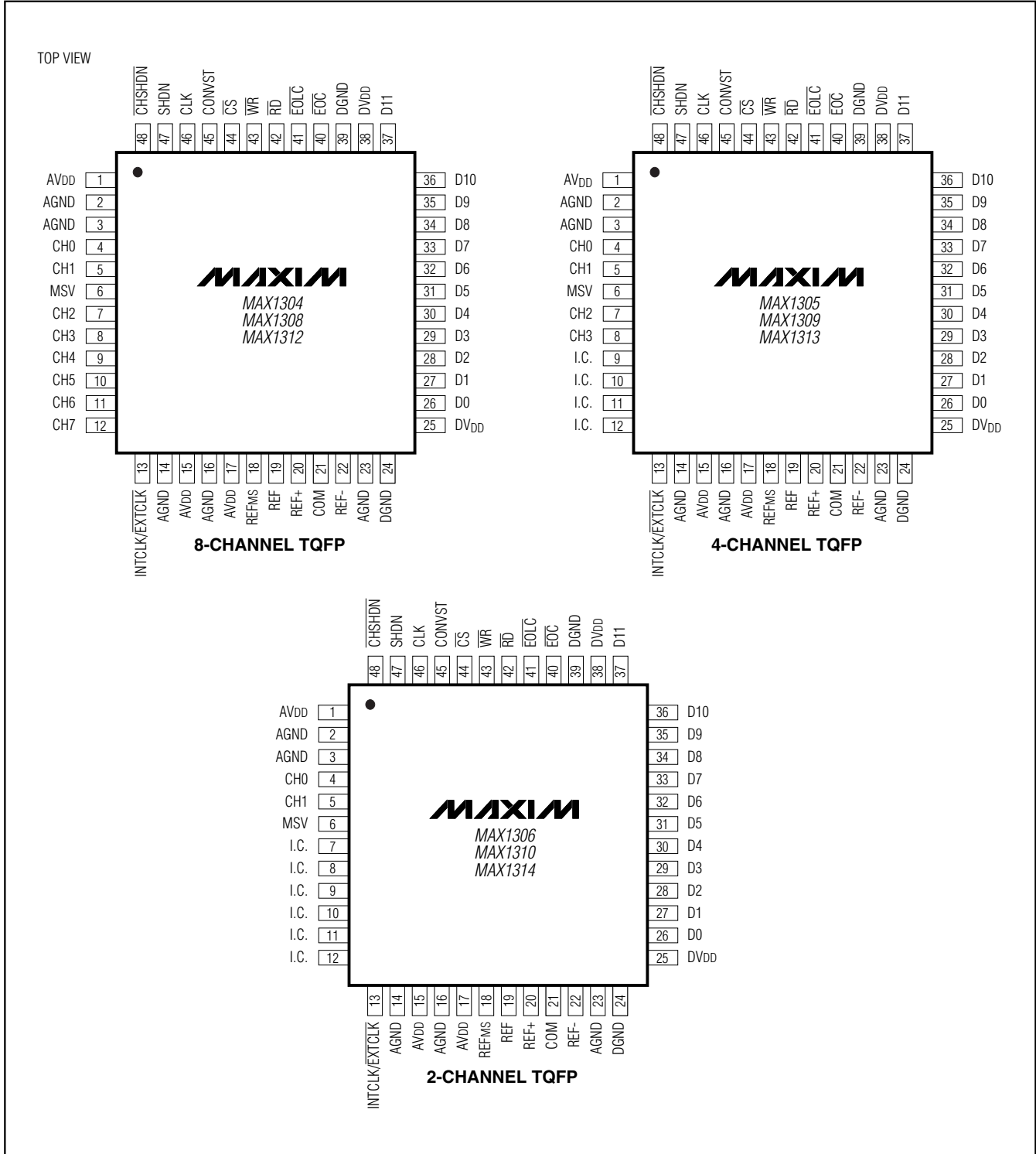
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PROCESS: 0.6 μ m BiCMOS

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with $\pm 10V$, $\pm 5V$, and 0 to +5V Analog Input Ranges

Pin Configurations

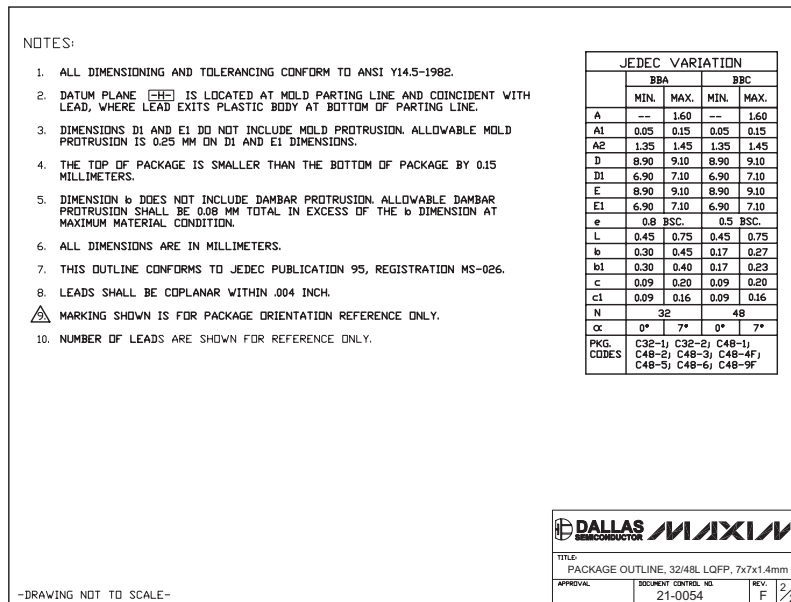
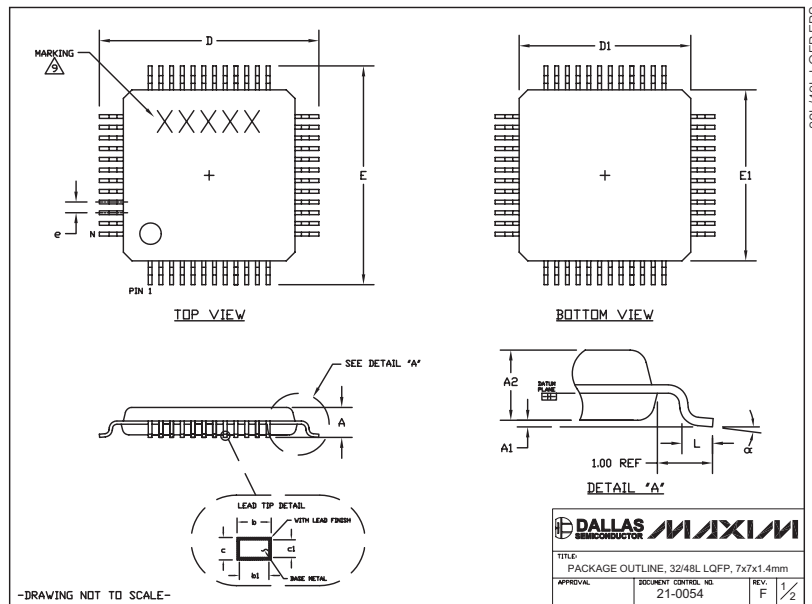
MAX1304-MAX1306/MAX1308-MAX1310/MAX1312-MAX1314



8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



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